N-type Organic Thin Film Transistors (OTFT): Effects of treatments of the insulator/semiconductor interface on the devices performances

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N-type Organic Thin Film Transistors (OTFT): Effects of treatments of the insulator/semiconductor interface on the devices performances

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To my husband

List of works

Journal papers

Electrical model for admittance spectroscopy in n-type thin film transistors
M. R. Fiorillo, R. Liguori, C. Diletto, P.Tassini, M. G. Maglione, P. Maddalena, C. Minarini,A. Rubino, in preparation

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Abstract

The organic electronic devices are finding a great consideration for applications where silicon limitations make this semiconductor unsuitable. Many properties of organic materials open new frontiers of the research; some example of applications are flexible displays, smart textiles, new lighting fixtures, intelligent packaging. Furthermore, an interesting attraction of organic devices is their being environmentally friendly. Organic materials provide also an inspiration for always new applications stimulated by the continuing efforts of characterization, fabrication, synthesis and design.

This thesis work wants to contribute to the comprehension of the properties of solution processed organic thin film transistors (OTFTs) that use a n-type semiconductor. These devices are the basic element of the driving circuits, where the n channel transistors still result poorly understood. In this PhD activity, it is studied the effect of surface treatments at SiO_2 dielectric layer and organic semiconductor interface to improve the OTFTs performance. These transistors, that are fabricated employing a specific combination of treatments before the deposition of a soluble semiconductor, are studied in order to analyze the relationship between the surface treatments and the devices electrical parameters; so to calculate one or more variables able to better adapt the conditions of the treatments to the performances of the device.

The devices are fabricated using as semiconductor the [6,6]-phenyl-C71-butyric acid methyl ester ($PC_{70}BM$) deposited from drop casting technique on a SiO_2 layer where a combination of ultraviolet/ozone cleaning (UV/O_3) and self-assembled monolayer (SAM) coating is previously carried out. The hexamethyldisilazane (HMDS) is the SAM used, and it is deposited at three different temperatures, 7°C, 25°C and 60°C. UV/O_3 cleaning allows to remove organic contaminations on the dielectric surface, thanks to the formation of hydroxyl groups (-OH) generated by the UV/O_3 ambient. While the HMDS can reduce the traps induced by Si-OH groups on the gate insulators, making layer treated hydrophobic. In this work, it is observed that different deposition temperatures of the SAM produce surfaces with different hydrophobic characters resulting in different electric performances of the devices.

The techniques of analysis employed to observe the effects of the treatments have been: contact angle measurements, AFM imaging of the organic semiconductor, *I vs. V* static characterization and admittance measurements.

Particular effort is given to evaluate the presence of electronic trap states in organic thin film transistors based on n-type semiconductor in bottom-gate bottom-contact configuration, thus it is proposed a new and accurate equivalent electrical, which is capable to model the properties of the semiconductor bulk and the conductive channel, through the calculation of the density of the trap states and the channel resistance.

From the performed analysis, the transistors treated at temperature of 25°C show a high roughness, a very inhomogeneous surface of the semiconductor layer and a higher degree of the SiO_2 surface hydrophobicity compared to the transistors processed at 7°C and 60°C. The HMDS behaving as a silane coupling reactant, provides a better tailored hydrophobic surface during the processes at 7°C and at 60°C, resulting in an improved surface energy, matching between the gate insulator and the organic semiconductor.

From DC measurements, it is observed that the samples at 60°C temperature for HMDS deposition show the best performances: the highest electron mobility of $13 \cdot 10^{-3}$ cm^2/Vs and the lowest threshold voltage of 12.0 V. While for the devices prepared at 7 °C and at 25 °C, the values of the mobility and the threshold voltage are $7.6 \cdot 10^{-3}$ cm^2/Vs - 13.6 V, and $2.8 \cdot 10^{-3}$ cm^2/Vs - 17.8 V, respectively.

The densities of the resulting trap states, calculated by admittance measurements and equivalent circuit, show the minimum quantity of the traps for the devices treated at 60°C compared to other devices, with a value of $1.48\ 10^{16}$ cm^{-3} eV^{-1}.

In conclusion, in this thesis it has been studied the effect of the deposition processing of HDMS layers on the behavior of $PC_{70}BM$ bottom-gate bottom-contacts OTFTs. In particular, the temperature of the HMDS process influences the quality of the semiconductor films and the devices performances. The hydrophobicity of the dielectric surface, induced by the HDMS process at 60°C, measured trough the value of the contact angle, which is of the order of 104.1° for this process, results in the formation of the highest quality of the $PC_{70}BM$ films, with homogeneous layers and a reduced quantity of traps, giving the OTFTs with the best performances. This results have allowed to develop a new equivalent electrical circuit, which, for the first time, models the AC behavior of bottom-gate bottom-contacts OTFTs with n-type semiconductors.

Introduction

The Organic Electronic devices have attracted large interest in the scientific community, as evidenced by the many groups of corporate and university research centers who work on these subject, including Philips, Samsung, Sony, but also the birth of associations such as OE-A (Organic and Printed Electronics Association), which includes more than 200 companies and research centers in the world, and promotes the creation of a competitive production infrastructure for organic and printed electronics.

Organic electronics is based on the combination of a new class of materials and large-area, high-volume deposition and patterning techniques. The peculiar mechanical properties of organics, the easiness of device manufacturing and the cheapness of the end products open the way to a wide range of applications, from flexible displays, to smart-card, up to wire devices for intelligent fabrics (smart clothing).

This technology is still in its early stage; while increasing numbers of products are available and some are in full production, many applications are still in lab-scale development, prototype activities or early production (Kirchmeyer et al., 2013).

The future of organic electronic is based on devices that are able to do things that are not possible for silicon-based electronics, expanding the functionality and accessibility of electronics, as the ability to create flexible and transparent devices. Organic electronic devices will be more energy-efficient than today's electronics, and will be manufactured using more resource-friendly and energy efficient processes than today's methods, contributing to a more sustainable electronic world.

Actually, many efforts have been done in order to develop the organic driving circuits, such as switches and memories, required for implementing a fully flexible, plastic electronics. In particular, for this aim, the interest is focused on solution processed organic thin film transistors (OTFTs) that could be the backbone of the plastic electronics.

A significant technological challenge is associated with the fabrication of organic complementary circuits, where deposition and patterning of the p- and n-channel semiconductors with high resolution is the objective pursued. The vast majority of organic complementary circuits reported in the

literature to--date are based on thermally evaporated p-channel/n-channel semiconductors. But, a proof of concept of the practical implementation of this technology in large-scale ICs is limited due to design constrains imposed by the shadow masks utilized for the semiconductor patterning. In this context, alternative deposition techniques (i.e. ink-jet printing, gravure printing, etc.) could potentially provide a long-term solution. In an effort to address this issue, significant research has focused on the organic semiconductors with useful solubility. As a result, a number of soluble p-channel semiconductors with carrier mobility comparable to amorphous silicon (a-Si) have been demonstrated and utilized in unipolar ICs. On the other hand, progress in the area of soluble n-channel semiconductors has been much slower with relatively few successful demonstrations. This distinct lack of soluble n-channel semiconductors has, to a large extent, hindered the development of large-scale organic complementary ICs (Wobkenberg & Anthopoulos, 2008).

In this context, this thesis work regards the fabrication of n-type OTFTs using the fullerene derivative [6,6]-phenyl-C71-butyric acid methyl ester ($PC_{70}BM$) as the semiconductor. This molecule is soluble in various organic solvents, allowing an easy deposition from solution and so being potentially much advantageous in the area of the large-area organic electronics.

The aims of the present research are the realization of n-type transistors with solution processed semiconductor to obtain good performance, as well as the understanding and the modeling of the mechanism involved in these unconventional materials.

A critical issue to be investigated in order to obtain good-performance OTFTs is the quality of the interfaces between the various layers constituting the device, particularly the interface between the semiconductor and the gate insulator, where the conductive channel is generated. For this purpose, in this work different processes are considered to improve the performance of the OTFTs, that are: the wafer cleaning procedures using an UV/O_3 treatment, the application of surfaces modification using a self-assembled monolayers (SAM), and different temperatures during the depositions of SAM layer.

Static electrical measurements and AC electrical techniques have been borrowed by the world of the inorganic semiconductors in order to evidence all the aspects regarding the features of the organic semiconductors and the devices based on them. DC measurements represent a basic tool for the analysis of the properties of organic semiconducting materials, while AC electrical techniques give the possibility of probing the local contributions to the observed overall properties showed by organics and devices, such as the limiting charge trapping phenomena due to extrinsic localized defects and the trapping produced by the intrinsic defects due to the structural features of the active organic materials, which are limiting factors in terms of OTFTs performance. To model these aspects, an electrical equivalent circuit was

proposed to interpret the data of the admittance measurements. This new RC network includes all the effects of OTFTs in bottom-gate bottom-contacts configuration and well describes the properties of dielectric/organic semiconductor (SiO_2/$PC_{70}BM$) interface.

In this context, the thesis work proposal regards the study of the interface and the related devices properties through the analysis of the grade of wettability of the dielectric surface after SAM deposition at different temperatures, the morphological analysis of the semiconductor layer in different conditions, and the application of both the methods of static and dynamic analysis of the electrical measurements.

The thesis is organized in five chapters. In the Chapter 1, it is presented a brief historical framework of the organic semiconductors, an overview on the principal features of the organic semiconductors and on their future applications. The Chapter 2 is dedicated to the organic thin film transistors, focusing the attention on ideal and non-ideal functioning principles, the devices architecture, the description of the extracted device parameters, the difference between p-type and n-type transistors, and possible new implementations of these devices. In the Chapter 3, it is described the fabrication process used to realize the samples and their analysis respect on some important parameters, as temperature and time. In particular, it is presented the architecture employed, the steps for the fabrication of the devices relatively to the description of UV/O_3 and SAM treatments, source and drain electrodes and deposition of the organic semiconductor. All activities carried out during the PhD activity are deal with in the Chapters 4 and 5. .

The experimental work was carried out at the ENEA Research Centre in Portici and in the Microelectronics Laboratory of the University of Salerno. All the fabricated devices have been processed in the cleanroom (class 100) located in ENEA, while the electrical characteristics are analyzed both at the ENEA and at University. The Chapter 4 is devoted to describe in detail the results of the experimental analysis to evaluate the fabrication processes adopted. Measurements of the contact angle and the semiconductor films morphology are part of this chapter. Furthermore, the results of the static characterizations of the OTFTs are presented. Thus, a part of the chapter is focused on the hydrophobic characteristics of the devices, with particular attention on the relationship between the grade of wettability and the devices performance. In the Chapter 5, the AC measurements of the devices admittance and a new model of the OTFTs AC behavior are presented. This model takes into account the devices geometry and the distribution of the traps levels in disordered semiconductors. The purpose of the proposed model is to evaluate the effect of the different treatments by extracting some interesting parameters that allow to compare them. Then, two models of the admittance associated with the traps are reported, together with fitting data and extracted parameters associated, respectively, to deepen the

understanding of the traps behavior in this type of semiconductors and devices. Finally, the AC parameters are compared with the resulting parameters of the DC measurements, to understand the efficacy of the treatments to improve the overall performance of the studied transistors.

Chapter I
Organic Semiconductors

In 1977 a new class of materials was discovered, their name was ‘conducting polymers’ (Shirakawa et al., 1977). These materials, now known as organic semiconductors, obtained significant interest of scientific communities in their properties and applications. This research consisted on the observation of increased electrical conductivity of halogen-doped polyacetylene, and for this work, Heeger, MacDiarmid, and Shirakawawere awarded the 2000 Nobel Prize in Chemistry.

In 1986 started the first applications of organic semiconductors: Tang reported a two-layer organic photovoltaic cell (OPV) using copper phthalocyanine (CuPc) and a perylenetetracarboxylic derivative as organic semiconductors (Tang, 1986) and, in the same year, an organic field-effect transistor (OFET) using polythiophene was first reported by Tsumura, Koezuka, and Ando (Tsumura et al., 1986). In 1987, Tang and VanSlyke realized organic light-emitting diodes (OLEDs) using an Alq3/diamine junction (Tang & VanSlyke, 1987). Even if the devices did not exhibit great performances, they were recognized as milestones about the electronic application of organic semiconductors, which lasts until present and is foreseen a very bright future.

The peculiarities of organics are given by their molecular nature, by weak intermolecular interaction. While for inorganic crystals all consisting atoms are strongly bound by covalent bonds, for organics the molecules are ‘weakly’ linked to each other by van der Waals force (Brown & Poon, 2004). Thus, this weak intermolecular interaction is responsible for the mechanical flexibility of the organic films or crystals. Furthermore, weak molecule-molecule bonds can be easily broken or reformed so molecules can be dispersed in solvents or evaporated at moderate temperature, allowing for various new process concepts for the organic semiconductors.

In this first chapter, it is shown a review on the fundamental physics and mechanism of charge injection into organic semiconductors (OSCs), and moreover a brief digression on defects and current and future applications.

Chapter I

I.1. Physics of Organic Semiconductors

Organic materials are characterized by building blocks made up by various forms of hydrocarbon (C-H) units, which can also include heteroatoms such as nitrogen, sulfur, oxygen, etc (Brown & Poon, 2004). For their typical energy gap ranges (between 1.5 eV and 3.5 eV) and their few mobile or free carriers at room temperature, organic materials can be considered as insulators. But the organic materials can be defined as organic semiconductors that exhibit semiconducting properties, and corresponding to a subset of a vast variety of organic materials.

Carbon is a chemical element in the fourth group of the periodic table, so it contains four valence electrons. The electronic orbitals of a carbon atom may hybridize differently, depending on the number of atoms with which the valence electrons are shared (Kymissis, 2009). The valence electrons can be shared with four neighboring atoms, to form four chemical bonds and four equivalent degenerated orbitals, referred to as sp^3 hybrid orbitals in a tetrahedral orientation around the carbon atom. Four sp^3 hybrid orbitals of equal energy are created by the superposition of one 2s and three 2p orbitals. It is also possible that only three chemical bonds are formed, so they have three coplanar sp^2 hybridized orbitals with one remaining p_z orbital. Three electrons of a carbon atom in the sp^2 orbitals are called σ-bonds, and are associated with a highly localized electron density in the plane of the molecule. The one remaining free electron per carbon atom resides in the p orbital, perpendicular to the plane of the sp^2 hybridization, to form so-called π -bonds (Fuchigami et al., 1993), (Matters et al., 1999). A schematic representation of the sp^2 hybridization and the formation of carbon-carbon double bonds is exemplified in Figure 1.

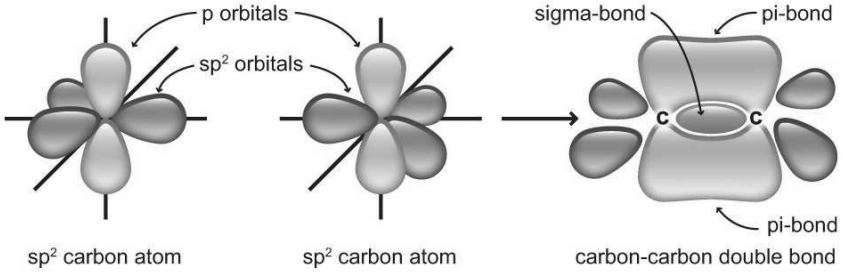


Figure 1: *Schematic representation of the formation of σ and π molecular orbitals from two carbon atoms with sp^2 hybridization.*

Due to the large overlap between the orbitals, σ bonds are strong and difficult to be broken because they have a high binding energy. Instead, the

π bond has significantly lower binding energy than the σ bond, because the distance between the two p_z orbitals is considerable, which means weak overlap or interaction between these orbitals; in this case, the electrons can be delocalized over several adjacent atoms. Thus, this weak π bond, or this delocalization of the electrons, makes it simple to displace electrons using an electric field, and then accounts for the semiconducting properties and the special characteristics of the organic molecules, as mechanical softness and solution-process compatibility that are the main advantages of weakly-bound molecules.

To describe the electronic energy levels, in the inorganic semiconductors, valence band and conduction band are considered, while for organic semiconductors exist similarly Highest Occupied Molecular Orbital (HOMO) and Lowest Unoccupied Molecular Orbital (LUMO). HOMO is the energy level at the top of a continuous band of occupied states, whereas LUMO is the first available energy level in the unoccupied band. The HOMO-LUMO gap is relatively small, due to the weak π binding energy. Therefore, organic materials can be considered as semiconductors due to the possibility to have a significant density of thermally-generated and/or photo-generated charge carriers. Delocalization of the electrons in the p_z (or π) orbitals implies the possibility of the movement of charge carriers inside a molecule, whereas the electrons forming σ bonds serve as a rigid frame that maintains the structure of the molecule. The electrons, loosely bounded and delocalized inside a molecule, are responsible for the electrical conduction. This type of chemical system where the π-electrons are delocalized through alternating single and double bonds is often called a π-conjugated system. In general, the σ and π bonds are defined intramolecular bonds which bind atoms to form a single organic molecule, while the van der Waals forces are the intermolecular interactions, that are very weak and the overlap of wave functions centered on neighboring molecules is very small (Schwoerer & Wolf, 2007).

I.2. Charge transport mechanisms

For the organic molecules, the fundamental property that allows for semiconducting properties at molecular level is the π conjugation. An example is the presence of alternating single and double bonds between covalently bound carbon atoms. Therefore, in organic solids, semiconducting properties at macroscopic level is only expected when the intermolecular interaction is significant, so that the π-electrons can have enough freedom to be delocalized and move from one molecule to another.

Because the intermolecular bonds in organic solids are due to relatively weak van der Waals interactions, the electronic wave functions usually do not extend over the entire volume of the organic solid, but are localized to a

finite number of molecules, or even to individual molecules. In this way, the charge transport through the organic semiconductor is limited by trapping in localized states, which means that charge carriers mobility μ in organic semiconductors is usually low and is expected to be thermally activated. Furthermore, most of the organic semiconductors are amorphous and rich in structural and chemical defects, therefore conventional models for charge transport must be adapted and extended; moreover, charges can move, with different mobility, within the molecular chain (intra-chain), between adjacent molecules (inter-chain), or between different domains, generally referred as grains (inter grain). The nature of the charge transport is still controversial, but several different models for charge transport in organic semiconductors have been developed, some of which will be discussed in the following.

The charge carrier transport mechanism can fall between two extreme cases: **band transport** and **hopping transport**. The band transport model assumes drift of charge carriers upon an applied electric field by repeated acceleration and collision with the lattice by which they totally lose their energy. This process is usually modeled by $\mu \sim T^n$ with $n > 0$ (Sze & Ng, 2007), where T is the absolute temperature. A temperature dependence of mobility is exhibited, along with a dependence on the applied electric field. In the band type conduction, electrons are scattered by lattice vibration, so that mobility decreases with increasing temperature, as illustrated in Figure 2(a).

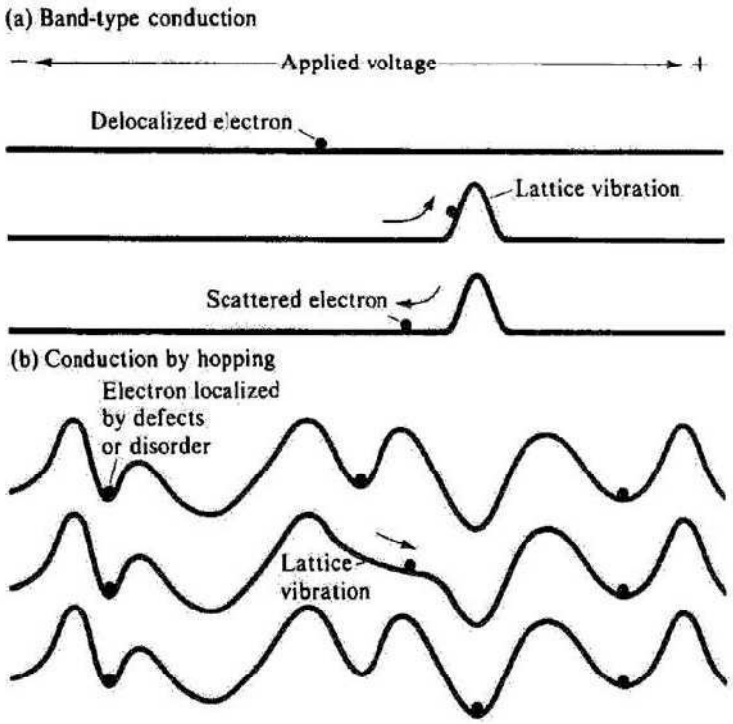


Figure 2: *Representation of the transport mechanism in solids with applied electric field, (a) for band transport conduction and (b) for hopping between localized states.*

The presence of the defects and the non-crystalline structure of the organic materials lead to the formation of localized states. In this case the transport can be described by **the hopping between** localized states. Transport is thermally activated as $d\mu/dT > 0$ because the lattice vibration helps localized charges to overcome potential barriers, Figure 2 (b).

Several charge transport models have been developed for the hopping motion. The **Poole-Frenkel model** (Frenkel, 1938) explains the increase of conductivity in insulators and semiconductor when high fields are applied. This model describes well the charge transport in many organic systems, and the charge carrier drift mobility has the form:

$$\mu = \mu_o exp^{(\beta_{PF}\sqrt{F})} \quad (1)$$

where μ_0 is the zero-field mobility, F the applied electric field and β_{PF} the Poole-Frenkel slope.

In the **model of variable range hopping (VRH)** the charge carrier is highly localized. In order to conduct, charge carriers hop between these localized electronic states by quantum-mechanical tunneling and overcome

the energy difference between them, emitting or adsorbing phonons during intra-chain or inter-chain transitions. In 1998, Vissenberg and Matters (Vissenberg & Matters, 1998) developed a theory for determining the mobility of the carriers in transistors with amorphous organic semiconductors. They pointed out that the transport of carriers is strongly dependent on the hopping distances as well as the energy distribution of the states. At low bias, the system is described as a resistor network, assigning a conductance $G_{ij} = G_0 exp\ (-s_{ij})$ between hopping site i and the site j, where G_0 is a prefactor for the conductivity and s_{ij} is defined as in eq.(2)

$$s_{ij} = 2\alpha R_{ij} + \frac{|E_i - E_F| + |E_j - E_F| + |E_i - E_j|}{2kT} \quad (2)$$

where k is the Boltzmann constant and T is the absolute temperature.

The first term in the eq.(2) describes the tunneling process, which depends on the overlap of the electronic wave functions of the sites i and j, E_F is the Fermi energy and E_i and E_j the energies of the sites i and j. In a lowest-order approximation, this tunneling process may be characterized by the distance R_{ij} between the sites and an effective overlap parameter α. The second term takes into account the activation energy for a hop upwards in energy and the occupational probabilities of the sites i and j. Starting from this expression, with the percolation theory, they can relate the microscopic properties of the organic semiconductors to the effective mobility of the carriers in a transistor. Specifically, carriers either hop over short distances with large activation energies, or over long distances with small activation energies. Since the hopping is thermally activated, the mobility increases with increasing temperature. With increasing gate voltage, carriers accumulated in the channel fill the lower-energy states, thus reducing the activation energy and increasing the mobility. The tunneling probability depends strongly on the overlap of the electronic wave functions of the hopping sites. This result is consistent with the observation that the carrier mobility is significantly greater in semiconductors characterized by a larger degree of overlap of the delocalized molecular orbitals of neighboring molecules. Thus, the mobility is dependent on temperature, gate voltage, and molecular arrangement in the solid state.

In contrast to the variable range hopping model, the **multiple trapping and release (MTR) model** was extended to organic semiconductors by Gilles Horowitz and co-worker (Horowitz et al., 1995). The model assumes that charge transport occurs in extended states, but that most of the carriers injected in the semiconductor are trapped in states localized in the forbidden gap, and that carriers cannot move directly from one state to another. These traps, that are associated with structural or chemical defects, can be *deep*, if their energy level is near the middle of the band gap, or *shallow*, if they are located near the conduction or valence band. An example of the distribution of these types of energy levels is shown in Figure 3.

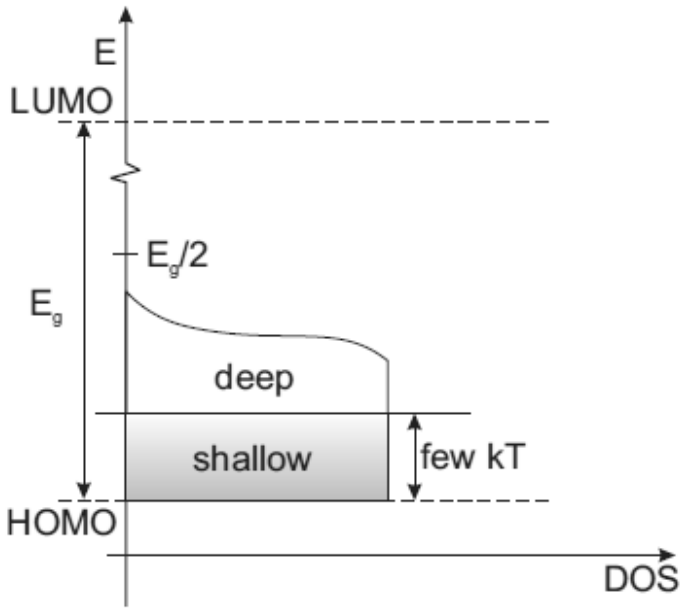


Figure 3: *Distribution of trap states in the band gap for a p-type organic semiconductor.*

Thus, carriers are temporarily promoted to an extended-state band in which charge transport occurs.

The model shows a dependence of the mobility of the carriers on temperature, on the energetic level of the traps, as well as on the carrier density and therefore on the applied voltage to a device. For a single trap level with energy E_{tr} the drift mobility is:

$$\mu_{D=}\mu_0 \alpha exp^{(-\frac{E_{tr}}{kT})} \tag{3}$$

whereμ_0 is the mobility in the delocalized band, α is the ratio of the effective density of state at the delocalized band edge to the concentration of traps.

Although the existence of an extended-state transport band in organic semiconductors, as postulated by the MTR model, is often debated, the MTR model appears to properly describe transport in organic semiconductors with a microstructure that favors a high degree of intermolecular orbital overlap, such as polycrystalline films of small-molecule and certain polymeric semiconductors with room-temperature mobility that approach or exceed 0.1 cm^2/Vs (Klauk, 2010). Indeed, quantum-mechanical calculations (VRH) of the charge-carrier dynamics in defect-free pentacene crystals suggest that carriers propagating through the molecular lattice under the influence of an

external electric field are delocalized over a significant number of molecule, and that the carrier drift velocity is within a factor of two of the saturation velocity in single-crystalline silicon (Hultell & Stafstrom, 2006).

Further theory for hopping charge transport is the **Gaussian disorder model** (GDM) proposed by Bassler (Bassler, 1993), and widely used for solids where the degree of disorder is high, where 'strong localization' results in the absence of extended band states. In this model, all electronic states have to be regarded as localized states, and their energetic distribution is described by a Gaussian distribution, Figure 4.

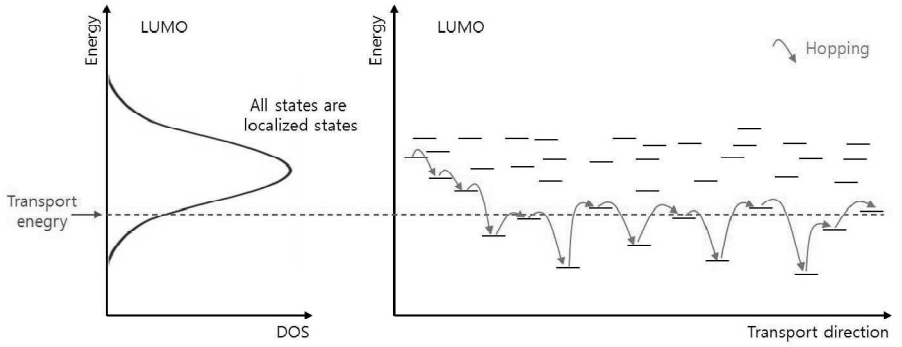


Figure 4: *Hopping transport through the localized states in the Gaussian disorder model (GDM).*

The major characteristics of this model are the non Arrhenius temperature behavior and the dependence of the mobility on the electric field. The expression for the GDM mobility can be written as:

$$\mu(F,T) = \mu_{\infty} exp^{\left[-\left(\frac{2\sigma}{3kT}\right)^2\right]} exp^{(\beta\sqrt{F})} \quad (4)$$

where μ_∞ is the high temperature limit of the mobility, σ is the energetic disorder, related to the half-width of Gaussian DOS (density of states) and β is a factor depending on the geometric randomness arising from structural or chemical defects.

Another model commonly believed to be suitable to describe transport mechanism in organic materials is the **grain boundary model** that explains the trap limited currents, which are presumably caused by traps located at grain boundaries. This model uses thermionic emission and assumes that charge states at the grain boundary present an electrostatic barrier to carrier transport, but charges within the grain screen the potential, reduce the barrier and increase the effective mobility (Steudel et al., 2004), (Shang et al., 2006) and (Verlaak & Heremans, 2007). The direct correlation of potential drops and grain boundaries has been visualized with Kelvin probe microscopy

(KPM) (Ohashi et al., 2007) and phase-electrostatic force microscopy (Annibale et al., 2007). Inhomogeneous voltage drops have further be seen for slightly contaminated gate oxides with KPM, while pure SiO_2 substrates show a homogenous voltage drop of up to 85% over the channel (Luo et al., 2007). Thermionic-emission over a Schottky contact barrier has also been used to explain the temperature dependence of the charge carrier mobility in rubrene single crystals, revealing two segments supposed to be described by the intrinsic polaronic transport above 150 K and the trap-dominated conduction below, resulting in a decreasing mobility with lower temperatures (de Boer et al., 2004).

I.3. Charge carrier injection

A physical behavior that strongly influence the amount of charge carriers injected into an organic semiconductor is the injection barrier at the metal electrodes/active layer interface. The barrier height strongly depends on the energy level matching between the Fermi level of the electrode material and the organic semiconductor energy levels, the HOMO or LUMO level of the organic semiconductor, for holes and electrons respectively.

One of the fundamental aspects of the metal/semiconductor interface is the Fermi level alignment, described by the Mott-Schottky model (Sze, 1981). When a neutral metal and a neutral semiconductor are brought in contact, the Mott-Schottky model predicts that their bulk Fermi levels align, causing the band bending in the semiconductor. In the Mott -Schottky limit, the vacuum level of the organic material and of the metal align, forming a region of net space charge at the interface, as depicted in Figure 5(a). However, the Mott-Schottky limit is rarely observed at real metal/organic interfaces due to the formation of a strong interfacial dipole Δ between the metal surface and the organic molecules, which tends to pin the Fermi level, Figure 5(b). The origin of the interface dipole is attributed to several mechanisms; charge transfer across the interface, formation of induced or permanent dipoles into the organic layer, chemical interaction, and presence of interface states (Miozzo et al., 2010).

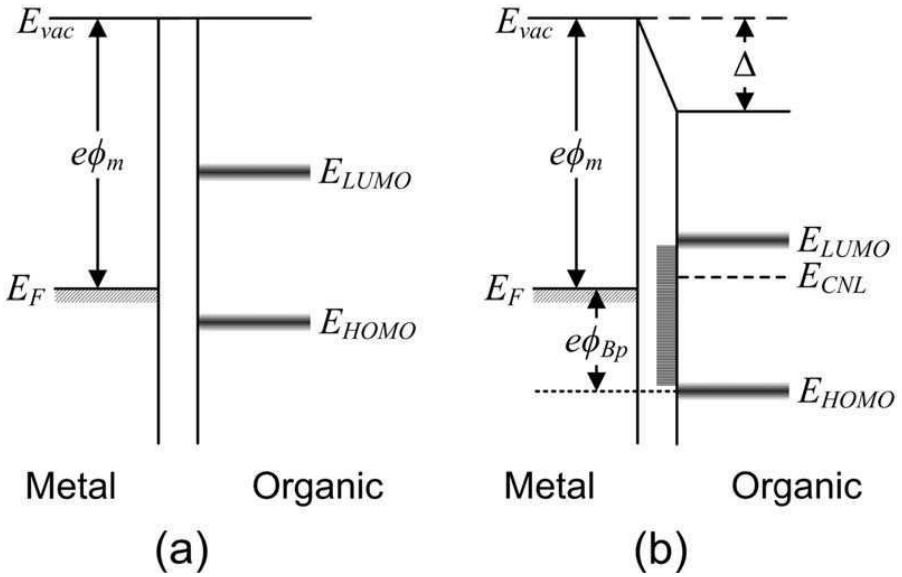


Figure 5: *Schematic energy level diagram of the band alignment at a metal organic interface, (a) Mott-Schottky limit vacuum level alignment, and (b) pinning of the Fermi level by induced interface states interfacial dipole.*

An effective metal work function $\Phi_{m,eff}$ can be defined as the difference between the pristine metal work function ϕ_m and the dipole(Helander et al., 2008),

$$\Phi_{m,eff} = \Phi_m - \Delta \tag{5}$$

For the inorganic semiconductors, Heine (Heine, 1965) demonstrated that surface states do not exist in the forbidden gap of most of them but gap states are induced in the semiconductor as a result of the rapidly decaying tail of the electronic wave function from the metal. These metal induced gap states are independent of the energy levels in the semiconductor, and hence can either be donorlike or acceptorlike when close to the valence or conduction bands, respectively. A charge neutrality level $E_{CNL}=e\phi_{CNL}$ is defined as the point at which the interface states are equally donorlike and acceptorlike. Therefore, at metal/semiconductor interfaces the charge neutrality level of the semiconductor will tend to align with the Fermi level of the metal as a result of charge transfer between the metal and the induced gap states, forming an interfacial dipole (Cowley & Sze, 1965),

$$\Phi_{m,eff} = \Phi_{CNL} + S_\Phi(\Phi_m - \Phi_{CNL}). \tag{6}$$

Here, the interface slope parameter S_Φ, for weakly interacting interfaces, was empirically found by Mönch (Mönch, 1987) to depend on the optical dielectric constant,

$$S_{\Phi} = \frac{1}{1 + 0.1(\varepsilon_{\infty} - 1)^2} \tag{7}$$

where ε_{∞} is the optical dielectric constant (high frequency limit of the dielectric function). Mott-Schottky model is generally used to choose the contact metal to not limit the performances of a device because of non-ohmic contacts. In the case where the density of interface states is very high, a Fermi-level pinning can take place, and the injection barrier becomes independent on the metal workfunction: it means that contact metal has no importance for the resulting injection barriers (Koch & Vollmer, 2006). This phenomenon accounts for an important implication for organic devices: they should generally bear a substantial injection barrier that cannot vanish below a certain level determined by the position of the pinned Fermi level.

Another important aspect that can have a strong influence in charge injection, is the presence of traps at the metal/organic interface, which are mostly produced during contact fabrication (Dimitrakopoulos & Mascaro, 2001). The deposition of the metal contacts can cause local damages in the structure of the material, due to the diffusion of the deposited specie into the active layer. On the other hand, the deposition of the organic material on top of the metal electrodes can lead to an accumulation of structural defects.

I.4. Defects in organic semiconductors

The electrical behavior of the organic materials is strongly influenced by the presence of trap states, which modify the number of the charges in the energy bands and the stability of the materials themselves. Charge carrier traps can be caused by structural defects or impurities. The structural defects are classified in: native point defects (as a vacancy), or interstitials, or extended defects (like edge dislocations, screw dislocations, or grain boundaries). Structural defects can lead to energy levels in the band gap. Some traps are electrically neutral when empty and become charged upon trapping a charge carrier. On the other hand, some defects are called antitraps because result in scattering centers, but do not cause traps (Klauk, 2006).

Organic materials are very sensitive to chemical impurities, which modify the number of the charges in the energy bands. In some cases, it is performed an artificial addition of chemical impurities which have different energy levels than the host material, and in Figure 6 is illustrated a simple scheme useful to understand the positions of electron and hole traps, respectively E_t^e and E_t^h, into a host material.

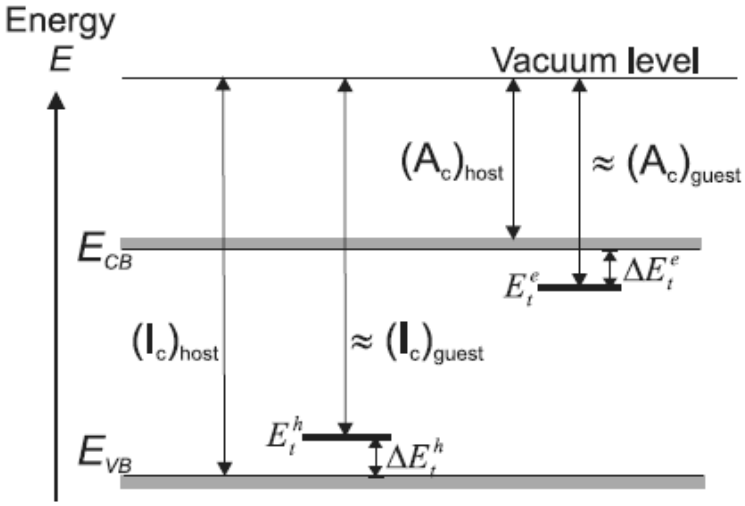


Figure 6: *Representation of the energy levels of a host material with chemical impurities* (Pope & Swenberg, 1999).

In Figure 6 ΔE_t^e and ΔE_t^h represent the traps depths for electrons and holes, while $(A_c)_{guest}$ and $(A_c)_{host}$ are respectively the electron affinity of the guest and of the host materials and $(I_c)_{guest}$ and $(I_c)_{host}$ are their ionization energies. The electron trap depth can be approximated with the difference in electron affinity of the host and guest materials and written as (Pope & Swenberg, 1999):

$$\Delta E_t^e \approx (Ac)_{guest} - (Ac)_{host} \tag{8}$$

In a similar way, the hole trap depth is described as:

$$\Delta E_t^h \approx (Ic)_{host} - (Ic)_{guest} \tag{9}$$

However, the atoms or molecules of the added impurity may deform the host lattice due to a different size, and may change the polarizability of the lattice in local. In presence of an impurity larger than the host molecule, a compression of the lattice and an increase in polarization energy result in the host, and traps located on host molecules adjacent to the chemical impurity. On the contrary, a small polarization energy results for a smaller impurity, so that the charge transport is impeded (Pope & Swenberg, 1999).

Defects can be introduced into materials also under ambient conditions, because of the presence of light, oxygen and water. For example, the adsorbed water on the gate dielectric can dissociate and react with organic semiconductor so that water molecules are able creating hydrogen bonds retained responsible of charge transport. An example of the oxygen effect on pentacene transistor characteristics is shown in Figure 7: a transistor is

measured as grown, kept in high vacuum, and after oxygen, that is the same device was measured after the oxidation process.

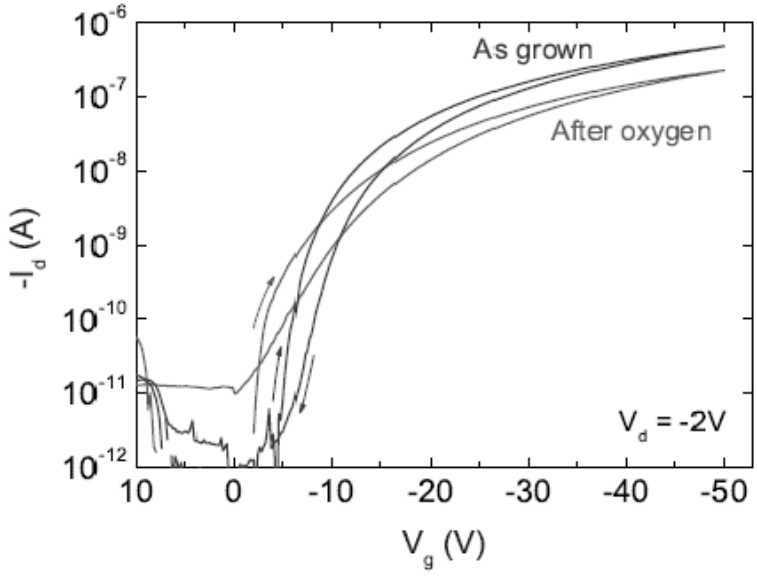


Figure 7: *Transfer characteristic of a pentacene transistor measured as grown (blue line) and after oxidation (red line). The graph shows the forward and the reverse sweeps in both cases.*

The characteristic oxygen effects on the transistor are a decrease in subthreshold performance, a decrease in on-current, and a shift of the transfer characteristic to more positive voltages, while the current hysteresis is essentially unaffected. Thus, these result in a decrease of the performances of the device, because the oxygen can cause changes of the flatband voltage in an organic semiconductor device. (Meijer et al., 2004), (Wang et al., 2006).

I.5. Organic electronics today and tomorrow

Electronic devices made with organic materials are being multiple applications and have been widely commercialized. Application areas of organic electronics can be grouped into five clusters, as shown in Figure **8**:

- Organic LED Lighting (OLED)
- Organic Photovoltaics (OPV)
- Flexible Displays
- Electronics and Components (printed memory and batteries, active and passive components)

- Integrated Smart Systems (ISS, including smart objects, sensors and smart textiles).

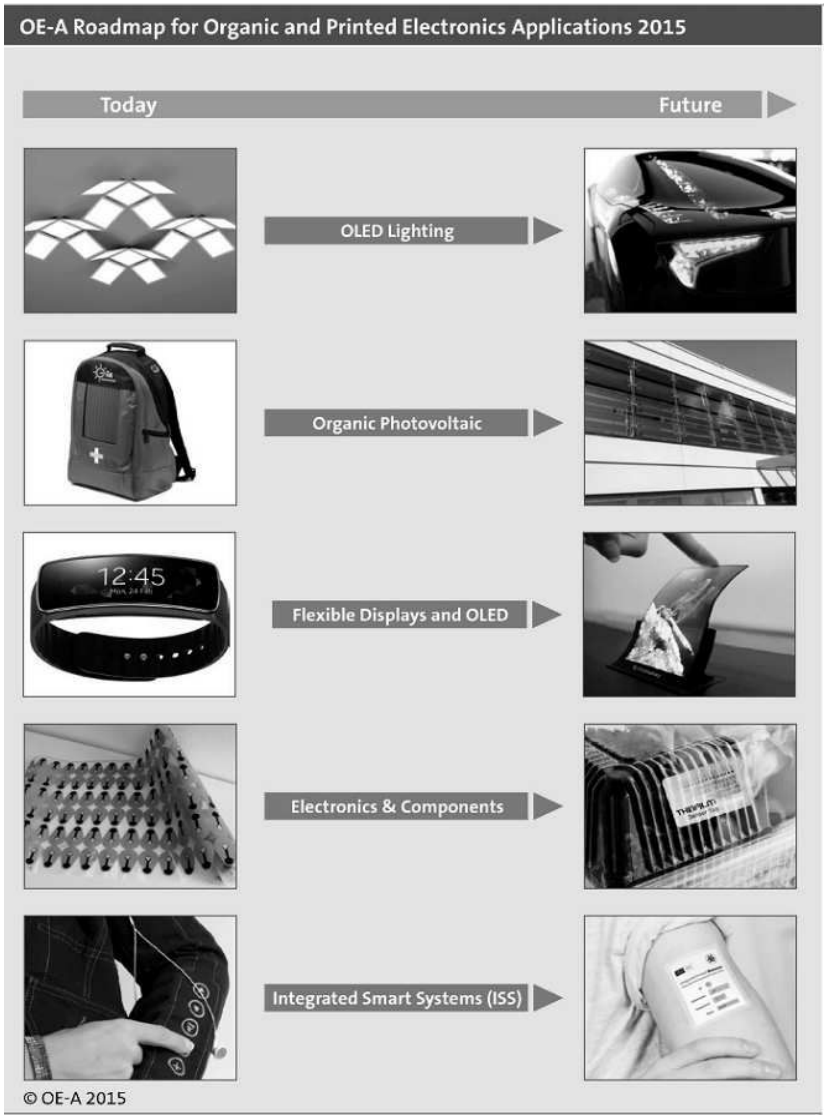


Figure 8: *Organic and printed electronics applications 6th edition of the OE-A roadmap(2015).*

Organic Display Technology and Organic light-emitting diodes (OLEDs) are commercialized in many smartphone models. For example, the Samsung Galaxy line of OLED-based smartphones occupies a significant portion of the global smartphone market. Additionally, Samsung and LG Electronics

have both announced forthcoming launches of large-screen OLED TVs. The new TVs are expected to not only be more spectacular than today's TV technology, with respect to crisper colors and sharper contrasts, but also lighter, thinner, and more energy efficient. Organic photovoltaics (OPVs), or organic solar cells, are generally viewed as one of most exciting near-future applications of the organic electronics, not necessarily as a replacement for silicon based PVs, rather because of the unique ways that OPVs can be used due to their flexibility, large-area coverage, and low cost. Current OPV technology boasts conversion efficiencies that exceed 10 percent, reaching even 12 percent, some researchers predict organic solar cells will reach 15-20 percent efficiency. However, even at this low efficiency, very interesting potential applications can be, for example, transparent films with solar cells on mobile phones or laptops to extend battery life considerably. Organic thin film transistors (OTFTs) are considered a fundamental "building block" of modern electronic devices, as amplifying signals and as on-off switches. OFETs are also highly sensitive to specific biological and chemical agents, making them excellent candidates for biomedical sensors and other devices that interface with biological systems. By 2020, with the synthesis of even more advanced materials, electronic mobility could increase to as much as 100 cm^2/Vs, while today values are at approximately $8 \div 11$ cm^2/Vs. Despite this progress, several challenges remain before OFETs will become a widespread commercial reality. For example, only recently researchers have demonstrated the fabrication of thermally stable flexible OFETs. High thermal stability is prerequisite to integrate OFETs into biomedical devices; otherwise they won't survive high-heat sterilization. In the future vision, numerous application possibilities for everyday use will arise thanks to the consistent refinement of organic electronics. It could be possible to illuminated wallpapers for room lighting or as a variant with an imprinted TV. Windows made of transparent solar cells could provide houses with energy. Screens and laptops could be printed and rolled. This technology will continue to grow, also thanks to the possibility to integrate organic devices in many systems of other technical sectors, changing the way society interacts with technological products, and for the future organic electronics applications there are hardly any limits to the imagination.

Chapter II
Organic Thin Film Transistors

Thin-film transistor (TFT) technology was developed by Paul Weimer in the 1962, using evaporated cadmium sulfide (CdS) as the semiconductor (Weimer, 1962). These devices are a special kind of insulated-gate field-effect transistors (IGFETs) made by thin films of materials. In 1973, the first TFT liquid crystal display (LCD) was demonstrated using cadmium selenide (CdSe) transistors (Brody et al., 1973). However, mass production of this kind of LCD on large-area substrates has never been realized. Among many possible reasons, there are complications in controlling the compound semiconductor thin film material properties and device reliability over large areas. The breakthrough in the TFT concept was achieved in 1979, using plasma-enhanced chemical-vapor deposited (PECVD) hydrogenated amorphous silicon (a-Si :H) (LeComber et al., 1979). Today, a-Si :HTFTs are widely employed as the pixel drive devices in active-matrix liquid-crystal displays (AMLCDs) on glass substrates (Street, 2007). The first organic TFTs (OTFTs) were reported only in the 1980s (Tsumura et al., 1986), (Kudo et al., 1984), (Clarisse et al., 1988). An organic TFT is fabricated by depositing thin films of an active semiconductor layer as well as the gate dielectric layer and the source, drain and gate metallic contacts on the surface of an electrically insulating substrate, such as glass or plastic foil. The total thickness of the devices can be less than50 nm. In this chapter, the characteristics of organic thin transistors will be analyzed. In particular, specific attention is paid on the working principles of the OTFTs, the possible architectures, typical organic semiconductor materials used in devices, and non-ideal electrical behavior of OTFTs. Finally, a brief digression on the evolution of OTFTs is presented.

II.1. Thin-film Transistor fundamentals

As said, OTFTs are a special kind of field-effect transistors (FETs) made by thin films (well below than 1 μm) of materials. A thin film transistor has

three terminals, named, as in a MOSFET, the source, the drain, and the gate (Figure 9).

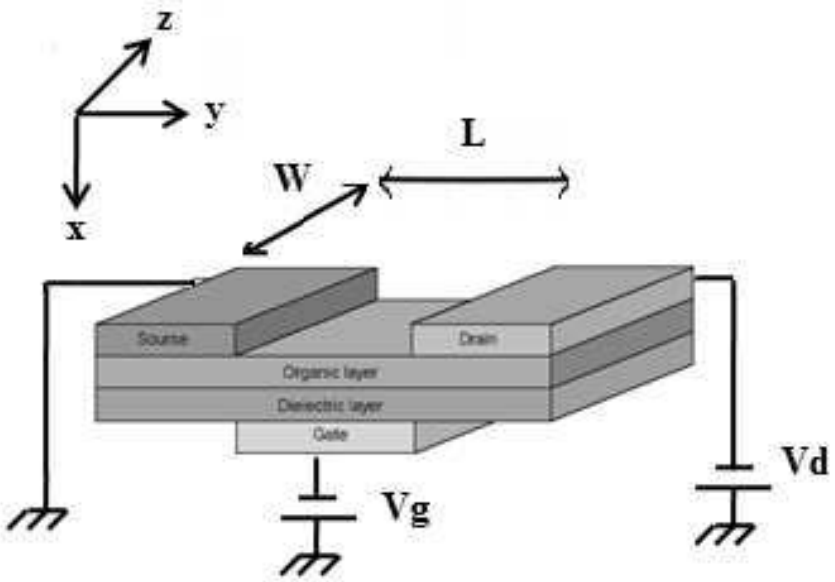


Figure 9: *Layer structure of an organic thin film transistor.*

A field-effect transistor operates as a voltage-controlled current source. A transistor controls the flow of charge between source and drain electrodes by applying a voltage across the gate dielectric, so that a sheet of mobile charge carriers is induced in the semiconductor that allows a current, the drain current I_D, to flow through the semiconductor when another voltage is applied between drain and source, Figure10.

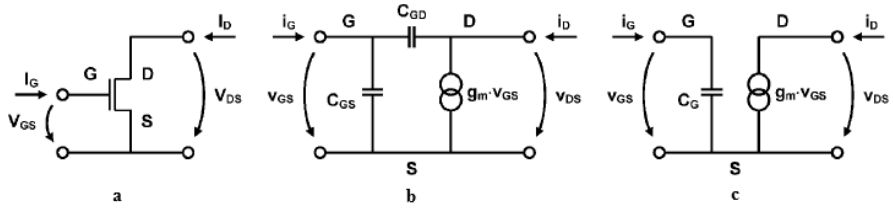


Figure10: *(a)Electrical symbol of a TFT, and (b and c) two small-signal equivalent circuits of a transistor, that show the gate-source capacitance C_{GS}, the gate-drain capacitance C_{GD}, the equivalent gate capacitance C_G, and the current source $g_m \cdot v_{GS}$*(Klauk, 2010).

In Figure 11 is shown the behavior of the energy-level diagram across the metal/dielectric/semiconductor interface of a p-type transistor. An organic semiconductor is defined to be p-type if the Fermi level is closer to the HOMO level than to LUMO, Figure 11 (b). Symmetrically, an organic semiconductor is defined to be n-type when the Fermi level is closer to the LUMO than to HOMO. Appling a positive voltage to the metal (the gate contact), depletion mode occurs in the p-type semiconductor, Figure 11 (c), and negative charges are induced at the electrode interface between the semiconductor and the insulator. On the contrary, when a negative voltage is applied to the gate, Figure 11 (a), holes can be accumulated at the interface between the insulator and the semiconductor. Considering this structure in an OTFT, source and drain electrodes are also present, and they are in contact with the semiconductor, Figure 11: the accumulated charges at the insulator-semiconductor interface form a conductive channel between these electrodes, which allows the charges to move between source and drain by applying a bias to them.

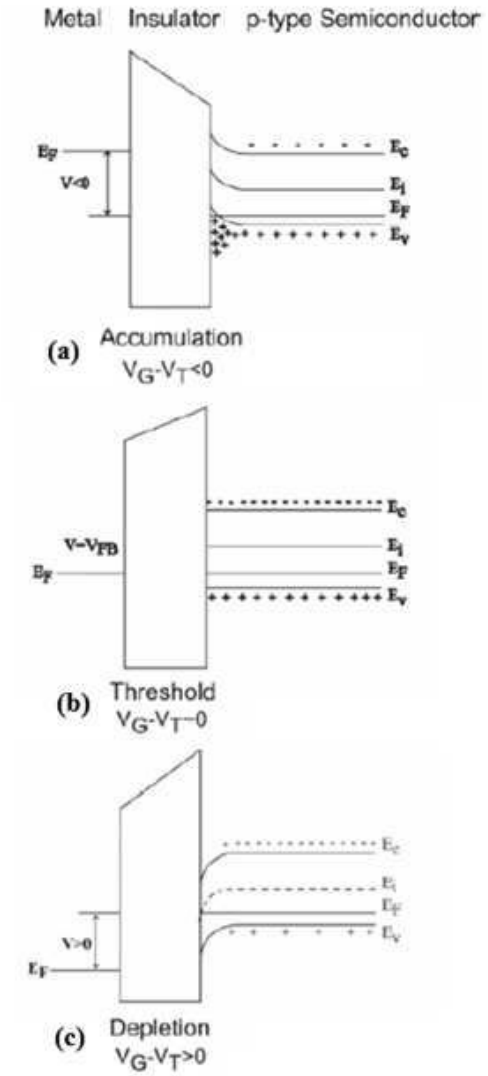
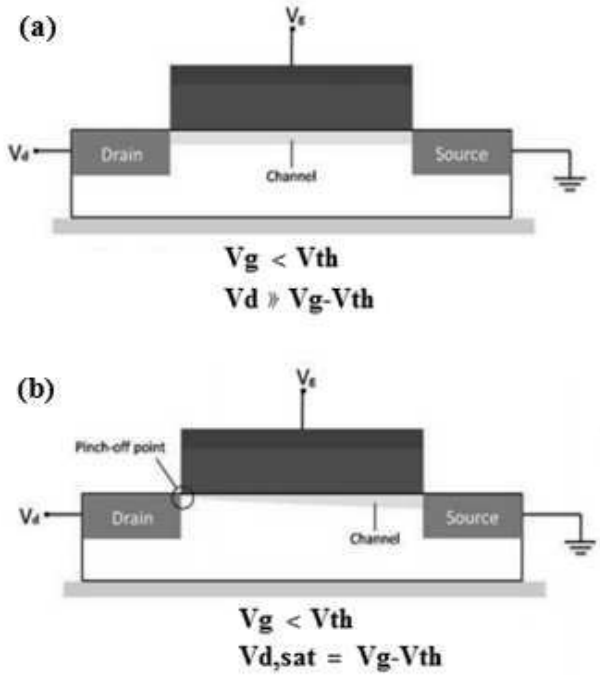


Figure 11: *Energy-level diagrams across the metal/dielectric/p-type semiconductor interface of an organic transistor, showing (a)accumulation mode, (b) flat-band mode, (c) depletion mode.*

OTFT electrical behavior is similar to a conventional FET that operates in the accumulation mode (Brown et al., 1997), Figure 12. In the semiconductor layer, the conductive channel is controlled by the gate and drain voltages, while the source electrode is grounded. The minimum gate voltage which can create the channel is called the threshold voltage, V_{th}. In the p-type transistor, when the gate voltage is lower than the threshold voltage, the device is turned on and in the channel results the accumulation

of positive charges at the insulator/semiconductor interface. In a real device however, not all the charges contribute to the current due to presence of traps and defects in the materials, where the charges are trapped.

The transistor operates in "linear regime" when low drain voltage is applied and the drain current is proportional to the drain voltage, Figure 12 (a). When the drain voltage is approximately equal to the difference of the gate voltage with the threshold voltage, a depletion region next to the drain contact starts forming and the channel is pinched-off, Figure 12 (b). The reason of the formation of a depletion region is that the potential difference between the gate and the drain electrode is above the threshold voltage in this case. Further reducing the drain voltage, the drain current does not increase through the transistor, but the depletion region broadens towards the source contact, Figure 12 (c), and this operation is defined as "saturation regime". The saturation drain current can flow across the depletion region due to the high electric field in this region, which induces charge carriers swept from the pinch-off channel to the drain electrode.



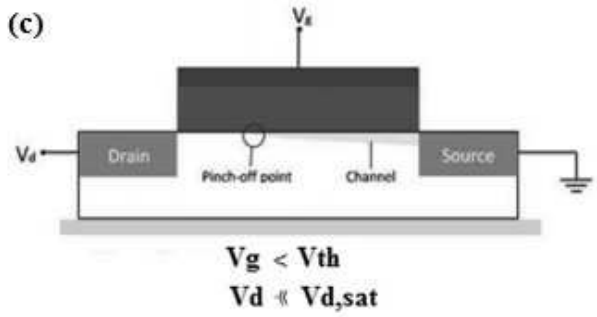


Figure 12*: Schematic operation regimes of p-type OTFT, (a) linear regime, (b) the start of saturation mode when the pinch-off point occurs, (c) the saturation regime.*

Another important aspect for the organic transistor is the choice of the material for drain and source contacts, as it provides a preferred injection or for electrons or for hole depends on the position of its Fermi level with respect to the frontier molecular orbitals (HOMO, and LUMO) of the organic semiconductor. The height of the injection barrier will be given by the difference between the contact Fermi level and the HOMO or LUMO level of the organic semiconductor, for holes and electrons respectively. According to this, gold is generally used for the realization of p-type organic transistors, because its relatively high work function (5.1 eV) forms a low hole injection barrier with the most common organic semiconductors. On the other hand, low work function metals, for example, calcium shows 2.9 eV, are generally used as electron injectors. But, these materials can be very reactive with oxygen and water vapor, so they need special care to be usefully employed.

Considering the metal-semiconductor interface, a Schottky barrier will be formed, as shown in Figure 13. As a voltage is applied between drain and source contacts, an off-current occurs due to the tunneling of charge carriers across the formed potential barrier (Figure 13 b). The potential barrier width can be reduced by applying a voltage to the gate electrode and, as a result, the drain current increases (Figure 13 c).

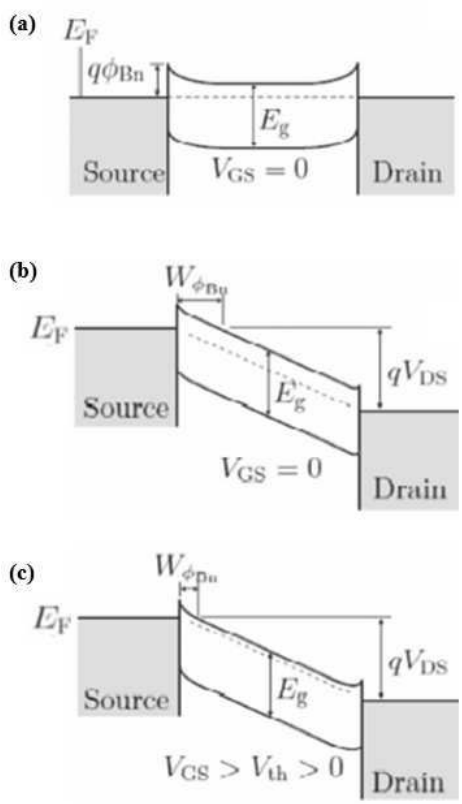


Figure 13: *Band diagram of the Schottky contacts to an n-type semiconductor with metal contacts: (a) without applied voltages, (b) with drain voltage only, and (c) with drain and gate voltages.*

Furthermore, organic materials are influenced by environmental conditions such as ambient humidity and oxygen. Water vapor and oxygen lead to modifications in the charge carrier field-effect mobility and in the threshold voltage (Cipolloni et al., 2007), (Jurchescu et al., 2004). To investigate the impact of ambient humidity and oxygen, long-term experiments are executed.

II.2. Architectures

The architectures of an OTFT depends on the sequence in which the three materials, semiconductor, dielectric and metal contacts, are deposited. The devices can be classified into two main groups, the staggered and the coplanar setup. The configuration is defined by the position of the S-D contacts and the gate dielectric compared to the channel area. In coplanar structures, in Figure 14 (b) and in Figure 14 (d), the drain/source electrodes

and the dielectric are located at the same side of the channel, whereas in staggered structures, in Figure 14 (a) and in Figure 14(c), the drain/source electrodes and the dielectric are placed at opposite sides. Furthermore, according to the position of the gate electrode and the metal contacts compared to the channel, the device can be represented in four different TFT architectures by their combination, Figure 14.

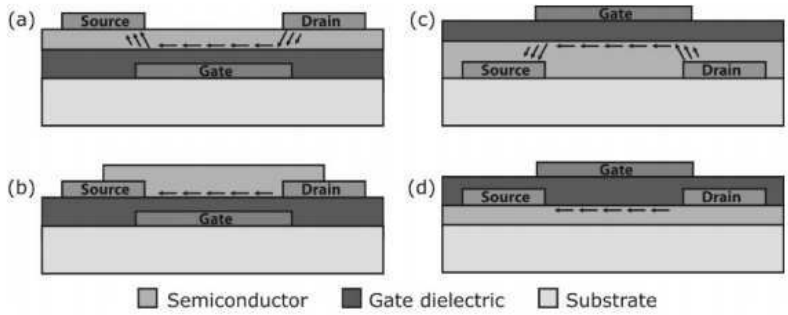


Figure 14:*General OTFT configurations: (a) staggered and bottom-gate top contact; (b) coplanar and bottom-gate bottom -contact; (c) staggered and top-gate bottom-contact and (d) coplanar and top-gate top-contact.*

The architecture strongly influences the device performance and the integration process. For example, in term of performance, experiments have shown that for the same energy barrier height, present at the interfaces between the organic semiconductor and the source and drain contacts, TFTs with a staggered structure (Figure 14 a, c) have the advantage of being less affected by this energy barrier than TFTs with a coplanar structure (Figure 14 b, d) (Gupta et al., 2009), (Shim et al., 2010). However, in case of the bottom-gate bottom-contact (BG-BC) (Figure 14 b), the effect of the energy barrier on the carrier exchange efficiency can be substantially reduced by modifying the surface of the source and drain contacts with a thin organic monolayer carrying an appropriate dipole moment (Cai et al., 2008), (Gundlach et al., 2008) or with a thin metal oxide (Kano et al., 2009), (Kumaki et al., 2008).

For the BG-BC, the gate dielectric layer and the source and drain contacts are prepared before the organic semiconductor is deposited. This is an important characteristic for applications require a high quality of the semiconductor, because semiconducting films are very sensitive to external perturbations; for example, electrical and structural properties can change if the OSC is deposited on a metal surface or not. As an instance, gold deposition on pentacene layer shows traces of metal diffusion in the OSC film, reducing the electrical potential barrier at the contact-channel interface (Tessler, 2001), (Watkins, 2002). Furthermore, the integration process has to

be adapted for the different setups. The BG-BC layout permits the semiconducting layer to be deposited in the last step of the process.

For this reason, the semiconducting film doesn't suffer from chemical impacts and other integration process steps. For example, pentacene films undergo a substantial drop in carrier mobility, if exposed to organic solvents, when those are employed for the solution-based deposition of polymer gate dielectrics and in photolithographic contact patterning processes (Gundlach et al., 1999). Whereas, for other configurations, the semiconductor has to withstand different processes, as for example lithography, etching or annealing steps. Deposition methods for metals, dielectrics, semiconductors and all materials used in the integration process should be also entirely suitable for specific electronic applications.

II.3. Materials

Organic semiconductors can be classified into two classes: polymers and conjugated small molecules materials (Facchetti, 2007).

The processing of the polymers is easy, because the possible deposition techniques can be solution processes. One of the main advantages of using a solution based process is the variety in coating methods. Most of the literature refers to spin-coating, drop casting, dip-coating methods; however, methods like inkjet printing, spray coating, doctor blade and Meyer rods have attracted the interest of research groups, due to the opportunity to integrate low-cost devices on large area and flexible substrates either using organic semiconductors (Yuan et al., 2014), (Diao et al., 2013). An example of a semiconducting polymer is poly(3-hexylthiophene) (P3HT), Figure 15.

Among the small-molecule organic semiconductors, the most widely studied materials include pentacene, sexithiophene and fullerene (C_{60}), Figure 15. Many small-molecule organic semiconductors are insoluble in common organic solvents, so they need to be deposited by sublimation in a vacuum environment. In most cases, small-molecule organic semiconductors readily self-organize into well-ordered polycrystalline films upon deposition.

Another classification of the organic semiconductors is based on their natural charge carriers: for p-channel semiconductors, the charges are holes, while for n-channel semiconductors, the charges are electrons. Most of the p-channel organic transistors have high stability in the ambient and in the bias applied conditions, whereas the n-channel organic transistors are usually unstable towards water and oxygen gas. So that many of n-type devices can be processed and analyzed in the inert or vacuum condition (Klauk, 2006).

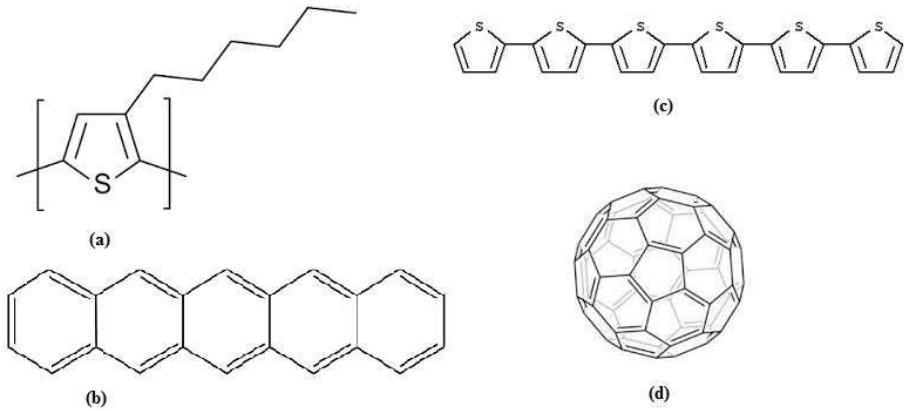


Figure 15: *Representation of a polymer: poly(3-hexylthiophene) (P3HT) (a), and of conjugated small-molecule organic semiconductors: pentacene (b), sexithiophene (6T) (c), fullerene (C_{60}) (d).*

During the last few decades, the more reported p-type material has been pentacene, because of its promising properties for organic transistor semiconductor applications. Nowadays, new materials with better environmental stability and higher mobility have been synthesized. Various research groups focus on materials such as dinaphtho(2,3-b:2′,3′-f)thieno (3,2-b)thiophene (Cn-DNTT) and 2,7-dioctyl(1)benzothieno(3,2-b)(1)benzothiophene (C8-BTBT), which can be deposited by thermal evaporation or from solutions, respectively (Zschieschang et al., 2011). Currently, the highest achieved field-effect mobility is about 43 cm^2/Vs for C8-BTBT deposited by a special off-centered spin-coating technique (Yuan et al., 2014).

The n-channel materials with electron mobility comparable to and even greater than that of amorphous silicon have been achieved in several material classes (Kanimozhi et al., 2012), (Zhan et al., 2011), (Zhao et al., 2011), despite the development of high performance organic electron-transport materials still lags behind that of hole transport materials to date. The fullerene is amongst the best performing electron transporting molecular semiconductors known to date, and electron mobility in the range of 5 cm^2/Vs has been reported (Li et al., 2012). This material is processed in vacuum, but a number of soluble fullerene derivatives, such as phenyl–C61–butyric acid methyl ester ($PC_{60}BM$) and [6,6]-phenyl-C71-butyric acid methyl ester ($PC_{70}BM$), have also been employed with solution deposition methods. Electron mobility can reach 0.21 cm^2/Vs (Chikamatsu et al., 2008), (Wobkenberg et al., 2008), but like C_{60} transistors, the performance of these devices degrades rapidly and substantially upon air exposure.

A graph of the remarkable improvement of mobility of the p- and n-type organic materials during the last years is shown in Figure 16. A continuous

growth is observed for both the types of materials, attributed to the unremitting advancements in the synthesis and fabrication processes. It is evident anyway that new materials are needed for higher performances.

Some studies have demonstrated that to increase the carrier mobility of many organic semiconductors, it is possible to grow the semiconductor films on low-energy surfaces (Lin et al., 1997). Self-assembled monolayers (SAM), such as octadecyltrichlorosilane (OTS) or Hexamethyldisilazane (HMDS), can induce low energy surface, but also the formation very small grains and therefore many grain boundaries in the OSC layer, so the semiconductor is distinctly three-dimensional. A method used to overcome this problem is the combination of the SAM with an inorganic dielectric, such as silicon dioxide: inorganic dielectrics are usually characterized by large surface energies favoring two-dimensional growth of the organic layer. Two-dimensional film growth typically results in large crystalline grains, and it was long believed that this was desirable to achieve good transistor performance (Klauk, 2010).

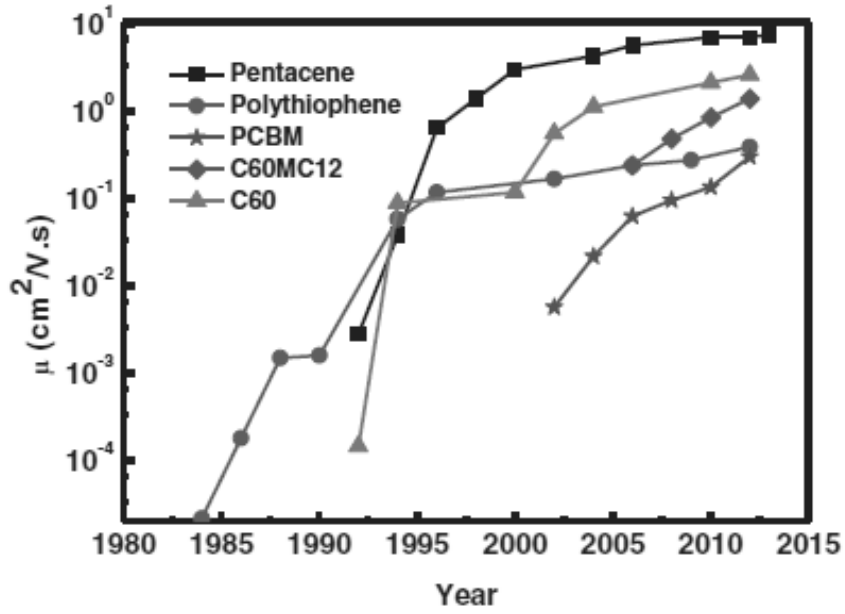


Figure 16:*Trend vs. time of mobility for some p-type (Pentacene and Polythiophene) and n-type organic semiconductors* (Kumar et al., 2014).

II.4. Operation Principle of OTFTs

The charges transport in organic TFTs is usually described with the same formalism of silicon MOSFET, remembering also that organic TFTs do not operate in inversion mode. Considering a p-type semiconductor as the active layer, the source and drain are electrically connected when to the gate it is applied a sufficient negative bias, V_{th}, and assuming constant the capacitance of the gate dielectric per unit area, C_i, through the channel; the charge quantity Q induced in the accumulation layer results to be equal to:

$$\mathrm{Q} = C_i \times \left[\mathrm{V_g} - \mathrm{V_{fb}} - \mathrm{V(y)}\right], \tag{10}$$

where V_{fb} is the flat-band voltage, that is the gate voltage which needs to be applied in order to enforce flat bands at the insulator-semiconductor interface Figure 11 b, and $V(y)$ is the potential difference of the semiconductor at a point y from the source electrode. But, the total charge consists of the charge induced in the accumulation layer and the intrinsic bulk charge Q_o in the semiconductor, where Q_o is defined as:

$$Q_0 = \pm q n_0 d_s, \tag{11}$$

where q is the elemental charge, n_o is the free carrier density, and d_s is the thickness of the semiconductor layer. The drain current is given using the following equation:

$$\mathrm{I_d} = \mathrm{W\mu[C_i(V_g - V_{fb} - V(y)) + qn_0 d_s]}\frac{\mathrm{dV(y)}}{\mathrm{dy}} \tag{12}$$

where W is the width of channel and μ is the mobility of the charge carriers in the channel.

Assuming a constant mobility, and defining the threshold voltage, V_{th}, as:

$$V_{th} = \left(\pm\frac{q n_0 d_s}{Ci} + V_f\right) \tag{13}$$

the drain current becomes:

$$I_D = \frac{W\,C_i}{L}\,\mu\left(\left(V_g - V_{th}\right)V_d - \frac{V_d^2}{2}\right), \tag{14}$$

which is valid for $|V_d| \leq |V_g - V_{th}|$, corresponding to the linear region of working of the device. L is the length of the channel. The quadratic V_d term in the eq. (14) is often neglected and so, in the linear regime, it results:

$$I_d = \frac{W C_i}{L}\mu_{lin}\left(V_g - V_{th}\right)V_d, \tag{15}$$

where the drain current linearly depends on the gate voltage, $I_d \, \alpha \, (V_g - V_{th})$, and on the drain voltage.

Increasing the drain voltage, the number of charge carriers tends to saturate and, near the drain, a point of pinch-off is established. For the $|V_d| \geq |V_g - V_{th}|$ condition, the drain current results:

$$I_{dsat} = \frac{W \, C_i}{2L} \mu_{sat} \left(V_g - V_{th}\right)^2. \tag{16}$$

The drain current in the saturation regime quadratically depends on the gate voltage, $I_d \, \alpha \, (V_g - V_{th})^2$, and is independent from the drain voltage. In both two regimes, the drain current can be modulated by regulating the gate-source voltage. This modulation is quantitatively described by the most fundamental field-effect transistor parameter, the transconductance g_m, the expressions for g_m in the linear and saturation regimes are:

$$g_{m,lin} = \left.\frac{\delta I_d}{\delta V_g}\right|_{V_g=const} = \frac{W \, C_i \mu}{L} V_d \tag{17}$$

for $|\mathrm{Vd}| \leq |(\mathrm{Vg} - \mathrm{Vth})|$,

$$g_{m,sat} = \left.\frac{\delta I_d}{\delta V_g}\right|_{V_g=const} = \frac{W \, C_i \mu}{L} \left(V_g - V_{th}\right) \tag{18}$$

for $|\mathrm{Vd}| \geq |(\mathrm{Vg} - \mathrm{Vth})|$.

By rearranging eqs. (15) and (16), expressions can be derived for the carrier field-effect mobility in the linear and the saturation regimes:

$$\mu_{lin} = \frac{L}{W C_i V_d} \frac{\delta I_d}{\delta V_g} \text{ for } |\mathrm{Vd}| \leq |(\mathrm{Vg} - \mathrm{Vth})|, \tag{19}$$

$$\mu_{sat} = \frac{2L}{W C_i} \left(\frac{\delta \sqrt{I_d}}{\delta V_g}\right)^2 \text{ for } |\mathrm{Vd}| \leq |(\mathrm{Vg} - \mathrm{Vth})|, \tag{20}$$

Figure 17 shows the typical electrical characteristics of a p-type organic TFT.

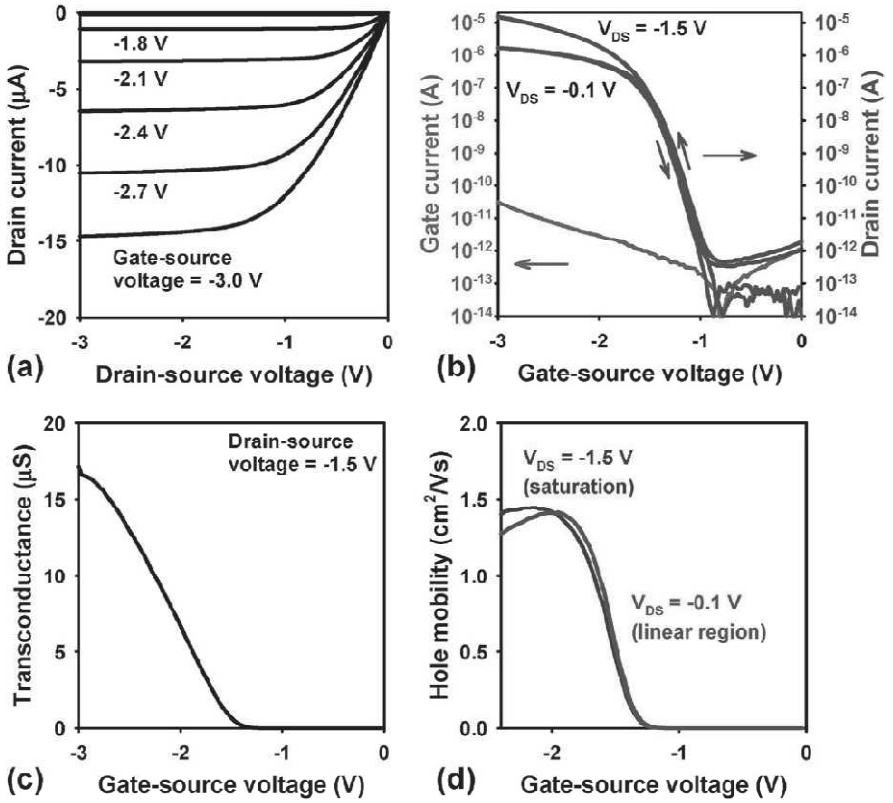


Figure 17:*Typical electrical characteristics of an organic p-channel TFT: output characteristics (a), input characteristics (I_g versus V_g) and transfer characteristics (I_d versus V_g) (b), transconductance g_m versus V_g (c), and carrier field-effect mobility in the linear and saturation regime (d),* (Klauk, 2010).

II.4.1. Transistor Parameters

To evaluate the performance of the organic transistors several parameters can be used: the carrier field-effect mobility, the threshold voltage, the sub-threshold slope, the on/off current ratio, and the stability (which can anyway be differently defined). These parameters are extracted from the electrical characteristic, in order to compare different devices.

The *carrier field-effect mobility*, μ, is the most important parameter for the organic transistors, because many parameters are correlated to it. Moreover, the choice of a semiconductor material is closely linked to high carrier mobility. The *threshold voltage*, V_{th}, is defined as the minimum gate-to-source voltage needed to create a conducting path between the source and drain terminals. Eqs.(15) and (16) describe the drain current above the threshold voltage. Below the threshold voltage, there is a working region in

which the drain current depends exponentially on the gate-source voltage. This is the sub-threshold region, and here the current is called *sub-threshold current*. In the sub-threshold region, the drain current is due to carriers that have sufficient thermal energy to overcome the gate-voltage-controlled energy barrier near the source contact and mainly diffuse, rather than drift, through the semiconductor to the drain contact. Another parameter referred to the sub-threshold regime is the *sub-threshold swing*, *S*. It is a measure of how easily a transistor can be switched from the off-state to the on-state and it is defined as (Sze, 1981):

$$S = \frac{dV_g}{d(\log_{10} I_d)}. \tag{21}$$

In addition to the threshold voltage, the *onset voltage*, $V_{on}(V)$, is a useful parameter. It is defined as the gate voltage where the drain current exceeds the noise level, which is typically at 10^{-12} A. The onset voltage and the flat-band voltage V_{fb} are approximately equal in many cases. Deviations may however exist in certain situations. Consequently, the trapped charge per unit area is approximately $C_i\,|V_{th}\text{-}V_{on}|$. The *total density of traps per unit are*a, $N_{\square}$ (cm^{-2}) can thus be estimated with (Goldmann et al., 2006):

$$N_{\square} \approx \frac{C_i|V_{th} - V_{on}|}{e}. \tag{22}$$

The *on/off current ratio*, I_{on}/I_{off} , is a parameter that indicates the ability of a device to shut down, that is to block the current flow. This parameter is the figure of merit for having high performance and low leakage power, relevant in the CMOS transistors and active matrix displays. The on/off ratio is extracted from a plot of I_d as a function of V_g in logarithmic, and it is taken as the ratio of the maximum current divided by the minimum current. Typically, more gate control leads to more I_{on}/I_{off} ratio. *Stability*, differently from other parameters, is referred to the variation of the OTFT performance parameters, such as V_{th}, μ, I_{on}/I_{off}, and *S*, versus other parameters such as time, temperature, light exposition, bias, etc., and it is profoundly affected by the purity, chemical sensitivity, and microstructure of the organic semiconductor film, but it is also a function of the details of the device operation, for example, how long the device is turned on at any given time.

II.4.2. Non- ideal transistor behavior

In organic transistors the electrical characteristics often deviate from an ideal transistor behavior. The approximation to linear transfer characteristics in the linear regime and to quadratic transfer characteristics in the saturation regime, is a method to extract the devices' parameters but the organic transistors show an ideal characteristic only in rare cases. Variations from ideal behavior are due to different factors, for instance depending on the

fabrication processes: irregular morphology of the semiconductor, mobile trapped charges in the dielectric and roughness of the semiconductor-gate dielectric interface. Non-ideal characteristics occur when the field-effect mobility varies with the gate bias. The issue is due to the charge trapping, and the relation with traps can be expressed as:

$$\mu = \mu_0 (V_g - V_{th})^{\gamma}, \tag{23}$$

where μ_0 and γ are semi-empirical parameters. Other non-idealities include contact resistance and leakage current (also called gate current). The contact resistance, R_c, depends essentially on the traps concentration, so that the drain voltage V_d doesn't drop only across the transistor channel but also at each interface between the source and the drain electrodes and the channel. The gate leakage current passes through the insulator layer. For organic materials, this undesirable current comes from the gate electrode, from source and drain contacts and in the channel area. A method to reduce this unwanted contribution consists in covering the gate dielectric with a thin film of a SAM (Klauk, 2010).

Another deviation by ideal OTFT behavior is the threshold voltage shift (TVS), (Matters et al., 1999), (Volkel et al., 2002) wherein prolonged device operation results in trapped charge at the dielectric/semiconductor interface, which subsequently modifies the threshold. A consequence of TVS is a hysteresis in I_d *vs.* V_d and I_d *vs.* V_g curves. Therefore, bias stress effects have a great impact on the application of organic semiconductors in electronic devices, limiting the reliability of the OTFTs. It is known that the bias-stress effect is reversible and that the recovery process can be enhanced by an inverse gate bias or by light (Libsch & Kanicki, 1993) (Kaneko et al., 1991). The operational stability of an OTFT can be quantified by measuring the time evolution of the threshold voltage shift verus time $\Delta V_{th}(t)$ during the application of a constant gate voltage. This dependence is described by a stretched exponential function characterized by the parameters τ and β according to:

$$\Delta V_{th}(t) = V_0 \left\{ 1 - exp\left[-\left(\frac{t}{\tau} \right) \right]^{\beta} \right\}, \tag{24}$$

whereτ is a relaxation time, β is the dispersion parameter, and V_0=V_g-V_{th0}, where V_g is the applied gate bias and V_{th0} is the threshold voltage at the start of the experiment. In analyzing threshold-voltage shifts in OFETs, β and τ are treated as fitting parameters. The higher the value of τ, the higher is the transistor operational stability, therefore τ is used as a figure of merit to compare devices fabricated using different technologies. An example of the characteristic of bias stress is shown in Figure 18.

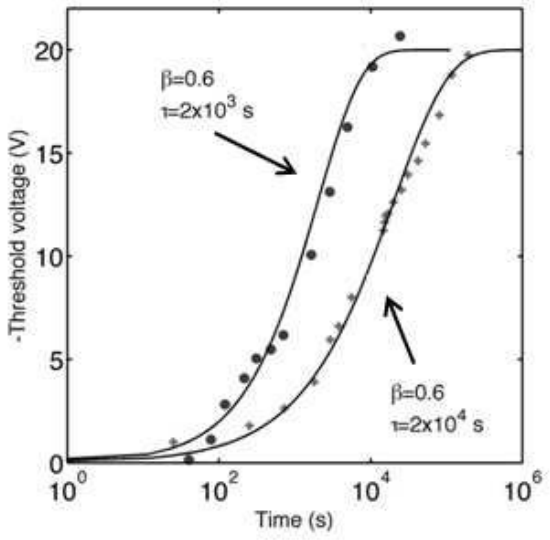


Figure 18:*Typical bias stress curves of two OTFTs.*

A principal cause of OTFTs instability, particularly for n-channel semiconductors, is their tendency to strongly interact with the constituents of the air, namely water vapor and oxygen. Many n-channel OTFTs show significant degradation in the performances when operated in air. This necessitates the device encapsulation, which introduces an undesirable extra processing step, and means that the OTFTs will anyway have a limited lifetime because the encapsulation is never perfect. De Leeuw and colleagues have considered the issue of the air stability in terms of the formal redox potentials for H_2O, O_2, and specific organic semiconductors (de Leeuw et al., 1997). The main problem is that the anions of the organic semiconductor molecules, which are formed at positive gate voltages, have large reducing power and can reduce or complex with O_2 and H_2O molecules that have diffused into the film. This means that the charged states of n-channel organic semiconductors are thermodynamically unstable in the ambient, therefore methods must be found (i) to prevent the diffusion of air into the active channel region (kinetic control), (ii) to limit the solubility of O_2 and H_2O in the film (thermodynamic control), or (iii) to block the chemical reaction between O_2 and the semiconductor molecules (chemical/kinetic control). The preparation of air-stable n-channel organic semiconductors still remains a major challenge (Newman et al., 2004).

II.5. Traps in OTFTs

A large traps density is the cause of some non-ideal behaviors of the OTFTs, as hysteresis effects, variations of the threshold voltage, non-ideal output or transfer characteristics, temperature dependence of the mobility and excess electrical noise. Traps may be caused by the dynamic motion of the molecules (McMahon & Troisi, 2010), (Sleigh et al., 2008), the grain boundaries (Himmelberger et al., 2013), impurities(Jurchescu et al., 2004), doping (Bussolotti et al., 2012), polar molecules (Nicolai et al., 2016) or through the interaction with the gate dielectric (Minder et al., 2012). Some traps can also be modified during or after producing the devices by thermal annealing (Puigdollers et al., 2010), exposing the organic semiconductor to gases (Sueyoshi et al., 2010), UV/O_3 or x-rays (Dacuna et al., 2014). The study of the traps is used to provide important information to improve the fabrication processes.

In organic electronics, trap concentration is often higher than the free carriers concentration. Traps are electronic states that can capture the free charge carriers in localized states, and the electrical transport takes place through hopping mechanisms. The trapped carriers can be released after a retention period, so inducing a reduction of the mobility of the material (Stallinga, 2009). These trap states are categorized into *shallow traps*, close to the respective transport level and *deep traps* further away from the transport level. The deep traps require a quantity of energy to remove an electron or a hole from the trap to the bands that is much larger than the characteristic thermal energy *kT*. The trapped charges are often considered as immobile charges, and their columbic charge influences the electric field distribution in an OTFT and then the charge transport: for instance, threshold voltage shifts are caused by immobile-trapped charge. However, if the release rate of the trapped carriers is sufficiently low, a significant time will be necessary to reach quasi-thermal equilibrium conditions. This causes delay and hysteresis effects in AC operated devices.

Many electrical techniques exist to detect the presence of the traps and their location in the device geometry, like: *small signal impedance spectroscopy* (IS), *thermal stimulated currents* (TSC), *electrical noise*. These methods can require the fabrication of dedicated devices such as Schottky diodes, metal-insulator-semiconductor (MIS) capacitors, or particular transistor configurations.

II.6. Evolution of the OTFTs

Organic thin-film transistors are considered to create a wealth of innovative opportunities for many electronic applications. OTFTs have several unique properties not shared by silicon transistors, the best known of all is the flexibility. For example, OTFTs have been fabricated on banknote

surfaces as an anti-counterfeiting feature, Figure 19 (a), because they are flexible enough that they can withstand repeated crumpling, creasing, and sharp folding. Furthermore, it is possible to embed them into the banknote paper, being the OTFTs structures thinner than silicon-based transistors: the OTFTs can achieve a thickness less than 250 nm, while the silicon substrates has a minimum thickness of about 20 µm (Chemical Sciences and Society, 2012). Other types of bendable applications are flexible displays, Figure 19 (b).

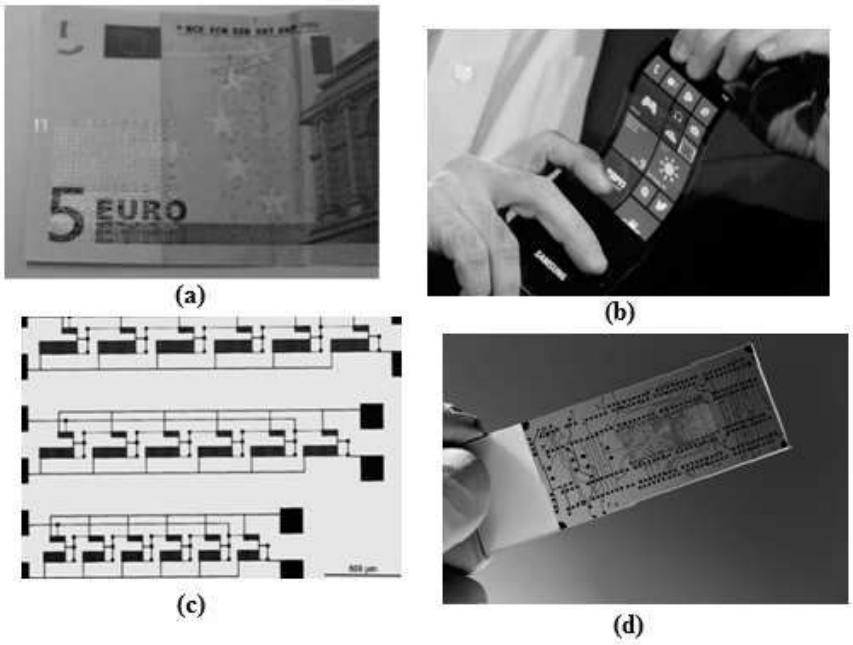


Figure 19:*Example of OTFTs applications: (a) banknote with OTFTs embedded as an anti-counterfeiting feature, (b) Samsung prototype of flexible display, (c) organic logic circuits made by ink-jet printing, (d) biosensor for flexible backplanes.*

OTFT technology is the best candidate for flexible display backplanes, due to the ability of the materials to withstand high strains without damage. Also logic circuit technology can use a similar fabrication process to flexible backplanes. NeuDrive is developing a range of logic circuit functions suitable for manipulation of electronic signals in a variety of applications, from healthcare to smart packaging. High mobility at short channel length has enabled ring oscillators with operating frequencies of over 600kHz to be achieved, making OTFTs a good candidate for logic applications where integration on flexible substrates is required. NeuDrive is one of the pioneers

of the development of ink-jet printed interconnections between transistors enable to create new circuits, Figure 19 (c).OTFTs are also highly sensitive to specific biological and chemical agents, making them excellent candidates for biomedical sensors and other devices that interface with biological systems, Figure 19 (d).

Despite much progress, several challenges remain, before organic transistors will become a widespread commercial reality. For example, only recently scientists have demonstrated the fabrication of thermally stable flexible OTFTs: high thermal stability is a prerequisite to integrating transistors into biomedical devices; otherwise they won't survive high-heat sterilization.

The potential future applications of OTFTs are many and varied, spanning across multiple fields: medicine and biomedical research, energy and the environment, national security, communications and entertainment, home and office furnishings, clothing and personal accessories, and more. Only by imagination and research is possible to overcome the current limits.

Chapter III
Fabrication of OTFTs

A critical issue of the Organic Electronics technology is to obtain n-type organic thin film transistors (OTFTs) with good performances and stability from the fabrication comparable to the p-type ones, in order to realize organic complementary circuits.

A fundamental contribution to the achievement of OTFTs with good performances is given by the quality of the interfaces occurring between the different layers in the devices (Fan et al., 2011), (Tiao et al., 2012). In particular, the interfaces between source or drain electrodes and the organic semiconductor influences the charge carriers injection, while the interface between the gate insulator and the organic semiconductor affects the carries conduction along the transistor channel. Furthermore, the devices behavior is significantly influenced by the microstructure of the active organic layer, which can be effectively tuned by different strategies, such as the wafer cleaning procedure (Song et al., 2010), (Qi et al., 2009), the deposition rate of the semiconductor layer (Shtein et al., 2002), the substrate temperature during the OSC deposition (Qi et al., 2009), (Shtein et al., 2002)and the interposition of a self-assembled monolayer (SAM) between the OSC and the underlying materials (Tiao et al., 2012), (Lee et al., 2008), (Liao et al., 2010), (Acton et al., 2011).

During the PhD activity, to have an insight on the behavior of the channel interface in n-type OTFTs as well as to target the improvement of these devices performances, different types of transistors were prepared, changing process technologies, materials and architectures.

The transistors were manufactured in a clean room ISO 5 (class 100) at the ENEA Research Centre in Portici. The n-type semiconductor analyzed was the fullerene derivative [6,6]-phenyl-C71-butyric acid methyl ester ($PC_{70}BM$), a soluble organic molecule. The OTFTs architecture was the bottom-gate bottom-contacts (BGBC) configuration.

To assure a good quality of the semiconductor layer, in terms of the crystallinity and the resulting charge carrier mobility (Yagi et al., 2005), before the deposition of the $PC_{70}BM$a combined process was applied, made

of a cleaning treatment, based on ultraviolet irradiation in ozone atmosphere, followed by the deposition of a SAM on the gate insulator.

In this chapter, a description of the experimental work performed during the thesis is reported. In particular, an overview of the fabrication, materials and methods that were employed to realize the OTFTs presented.

III.1. Architecture of the devices

The BGBC topology was chosen to prepare the OTFTs because it is the most convenient one from an industrial standpoint, as it allows to fabricate complex circuits and sufficiently small structures able to produce channel lengths shorter than a few tens of micrometers and obtain large-scale integrated systems. Furthermore, the electrical and structural properties of the semiconducting films can change and degrade when other process steps are performed after their deposition. It is therefore desirable to use a BC configuration for promising applications such as high-resolution flexible displays and device's printing applications (Xu et al., 2007).

The $PC_{70}BM$-based OTFTs were fabricated on commercial substrates, dimensions 10 mm X 10 mm X 0.5 mm, Figure 20. The gate contact is made of heavily doped n-type silicon, with 200 nm thick SiO_2 as the gate dielectric. It was chosen a silicon substrate, material with known characteristics, to increase the performances of electron transporting semiconductor deposited via solution processing, that nowadays is a significant challenge. Source and drain electrodes are made of interdigitated gold contacts, thickness 50 nm, with 5 nm of chromium as adhesive layer on the SiO_2. The pattern is composed by four devices with two geometries, one characterized by a channel width *W* equal to11.2 mm (devices A and B) and the other with 22.4 mm (devices C and D), while the channel length *L* is 20 μm or 40 μm, respectively, giving thus a *W/L* ratio constantly equal to 550.

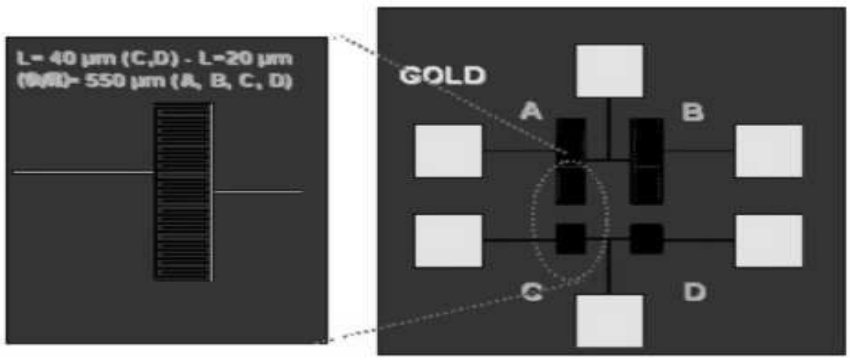


Figure 20: *(right) Substrate layout and (left) magnification of the interdigitated fingers, with the specifications of the channel devices.*

Interdigitated contacts are used in order to both obtain high values of the ratio *W/L* between the width and the length of the channel(so avoiding the short channel effect) and miniaturize the device active surface. This structure is used to OTFT tester, starting point for the optimization of the layer of the semiconducting material, which can be deposited by solution or by evaporation process.

III.2. Fabrication of the OTFTs

The fabrication of the devices was realized in clean room, ISO 5 (class 100), at the ENEA Research Centre in Portici. The clean room is an environment with a controlled level of contamination, that is specified by the number of particles per cubic meter at a specified particle size. During the performed processes, the temperature of the clean room was 21°C, while the detected humidity was 50%.

The steps to manufacture the devices for this PhD thesis were:

- cleaning of the SiO_2surface using an UV/O_3 treatment,
- deposition of the SAM (namelyhexamethyldisilazane(HMDS)) at different temperatures: 7°C, 25°C, 60°C,
- annealing of the samples for 1 h at 100°C in inert atmosphere,
- deposition of the $PC_{70}BM$ by drop casting technique from chlorobenzene solution (2 wt%) at room temperature in inert atmosphere,
- solvent evaporation from the $PC_{70}BM$ films in inert atmosphere.

The deposition of the devices' active layer (semiconductor) took place inside a glove box. This is a sealed container, designed to allow to the manipulation of objects inside a closed environment where it is present a controlled atmosphere, separated from the external one. The control usually targets to have a chemically inert atmosphere inside the box, so(i) using pure nitrogen,(ii) monitoring and reducing the presence of water vapor and oxygen continuously recirculating the nitrogen through active filters and reactors, and (iii) keeping the inside pressure above 1 atm. During this particular experimental phase, inside the glove box H_2O <1 ppm and O_2<1 ppm were measured. So that, the manipulation of the substances is done within a very high pu

re inert atmosphere. To reduce as much as possible the presence of water and oxygen contamination at the interface OSC-dielectric is an important factor for the good behavior of the n-type organic transistors, because n-type OSCs usually chemically react with the atmospheric oxidants (e.g. water, oxygen), so degrading their performances (Anthopoulos et al., 2006), (Yu et al., 2013).

The cross-section of the OTFTs is shown in Figure 21.

The HMDS deposition was done by vapor phase at three different temperatures: 7°C, 25°C, 60°C, keeping the samples and a reservoir of the HMDS inside a sealed container. For the deposition at 7°C, the container is maintained inside a refrigerator for 4 days; the samples at 25°C are processed for 1 day; and the process at 60°C is performed for 1 day using a hot plate.

The duration of the deposition process of the HMDS for the different temperatures was selected after a preliminary observation of the results obtained from the contact angle measurements for the various treatments in temperature. Initially, all the devices were processed in one day (24 h). However, the treatment at 7°C was found to induce a degree of wettability still hydrophilic, with a small increase of the CA respect to the UV/O_3 treatment only. The resulting AC values were not comparable with the ones calculated for the devices prepared at the other two temperatures. This can be due to a small evaporation rate of the HMDS and to a low energy of the HMDS deposition process at low temperature, which cause a slower formation of the SAM. In addition, it was observed that CA for HMDS processes longer than 4 days didn't further change. For these reasons, the duration of the HMDS process at 7°C was chosen of 4 days.

In the following paragraphs, the various process steps are described and explained the choices made.

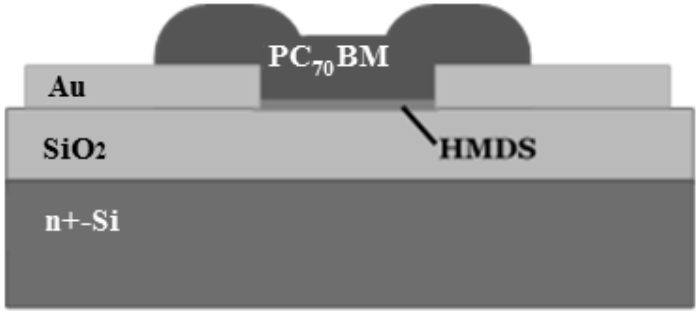


Figure 21:*Schematic representation of the bottom-gate, bottom-contact (BGBC) transistor architecture used.*

III.3. Cleaning of the SiO_2 surface with UV/O_3 treatment

For a bottom-gate OTFT, the quality of the OSCs is very sensitive to the conditions of the surface of the gate insulator. Many surface treatments exist to improve the surface property of the dielectric, and enhance the electrical performances of the devices(Susukida et al., 2007), (Guo et al., 2006). Some of these are UV/O_3 treatment and plasma oxidation.

In this study, the UV/O_3 treatment (or cleaning) was used. It is a cheap and simple method, Figure 22, which can remove the organic contaminants

from the surfaces. The cleaning effect is caused by irradiating the surface of a substrate with suitable lamps creating enough energy in the Ultra Violet spectrum range, inducing the formation of atomized oxygen and then of highly reactive ozone inside the system. Furthermore, on the surface the UV radiation stimulates the reaction of the organic compounds with the ozone, and their conversion into volatile substances, for example H_2O, CO_2, N_2, easily removed from the system (Vig, 1985).

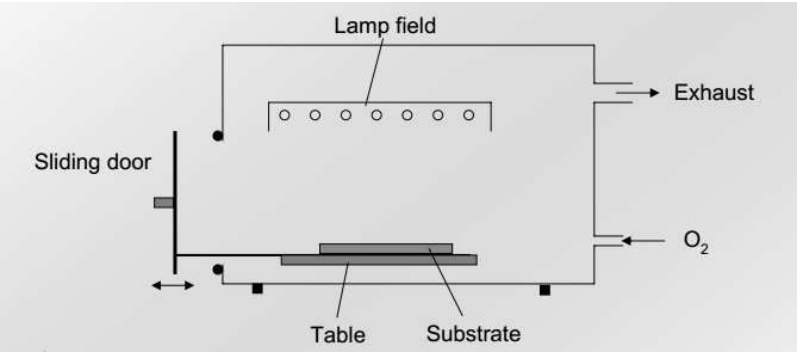


Figure 22:*Description of a UV/O_3 surface treatment system.*

Although the OTFT samples treated with UV/O_3 process show significant improvements in the morphology of the OSC and in the electrical characteristics of the devices, the treatment time must be calibrated in function of the contaminant and on the organic OSC used. This could depend on the number of the hydroxyl groups (-OH) generated by the UV/O_3 ambient on the insulator surface, resulting in a more or less hydrophilic insulator surface, which would affect the growth quality of the semiconductor channel film, and the interface traps density at the surface (Koo et al., 2009), (Wang et al., 2006).

In this thesis, the process was performed in a system MBRAUN UV-O_3 OP73, and the substrates were exposed to the treatment for 20 min. This time was selected after performing some preliminary tests, using three exposure times:5 min, 10 min, 20 min. The devices prepared on the samples treated for 20 minutes showed the best performances in terms of mobility and threshold voltage. This is due to more hydrophilic insulator surfaces, prior to the SAM deposition, which caused an improvement in the growth quality of the OSC and thus enhanced the electrical performances of the devices. Processes longer than 20 min didn't give better performances.

III.4. Surface Treatments of Self-Assembled Monolayer (SAM)

An interesting approach for OTFTs with the bottom-gate structure is the use of a thin oxide layer SiO_2in combination with a high-quality insulating organic self-assembled monolayer on top of it (Fan et al., 2011). As described in paragraph II.3, to improve the mobility of the organic semiconductors, it is possible to combine inorganic dielectrics, which have large crystalline grains but large surface energies, with SAMs that present low-energy surfaces but also small grains and significantly grain boundaries. The use of SAM gate dielectrics for organic TFTs was pioneered by the Vuillaume group (Collet et al., 2000). They investigated the mechanism of carrier transport through SAMs despite their thickness of only a few nanometers.

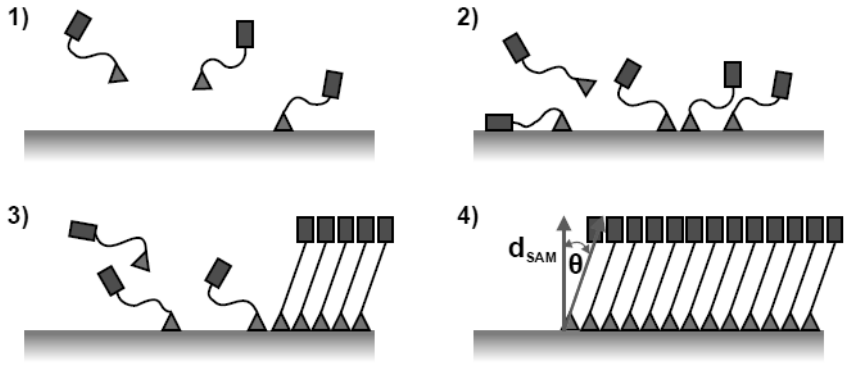


Figure 23: *Formation mechanism of a generic SAM.*

A scheme of the formation mechanism of the SAMs is illustrated in Figure 23. SAM molecules are composed of three building blocks: (i) an anchor group(green triangles in the image), with a distinct affinity to the target surface, controlling the adsorption by chemical or physical interaction to the adsorbent surface; (ii) a hydrocarbon spacer chain(black connecting lines), regulating the intermolecular interaction and contributing to the ordering; and (iii) a terminal functional head group(blue rectangles), determining the surface properties of the SAM (Luschtinetz et al., 2010).

In the first step of the layer formation, the molecules are transported through a combination of diffusive and convective transport to the substrate surface (Schwartz, 2001), Figure 23 (1). These are adsorbed and randomly distributed on the substrate surface, because of the interaction between the substrate and the head group of the adsorbate molecule, Figure 23 (2). In the third step, the nucleation and formation of domains with densely packed molecules and uniform orientation are due to surface diffusion and

intermolecular forces. In this step, there are both amorphous regions and ordered regions that continue growing and that will cover the whole substrate, after a certain period of time. The self-assembled monolayer is defined by the layer thickness, d_{SAM}, which in turn is determined by the molecule length and the tilt angle θ between the molecular axis and the surface (Schreiber, 2000), Figure 23 (4). Remaining defects in the SAM can be compensated by prolonging the deposition time or by a subsequent heat treatment after the deposition.

The formation of the SAMs is based on two steps. The first has a duration of a few minutes and the SAM thickness reaches 80 ÷ 90% of the final one. Following the diffusion-controlled Langmuir adsorption, that depends on the concentration of the SAM solution, the kinetics of this process is regulated by the interaction of the anchor group. The second step is slower, with durations of hours or days, and it involves ordering or surface crystallization with accompanying rearrangement of alkyl chains and it is more dependent on the interactions between the organic chains, such as dipolar and van der Waals interactions, and the degree of disorder (Ulman, 1996).

The self-assembled monolayer used in this work was HMDS hexamethyldisilazane ($[(CH_3)_3Si]_2NH$), Figure 24. The monolayer of this material can be prepared from solution(Collet et al., 2000), (Majewski et al., 2004), (Ha et al., 2009), from the vapor phase(Dibenedetto et al., 2009), (Dibenedetto et al., 2008),or by microcontact printing (Zschieschang et al., 2008). In this work, the HMDS is deposited by vapor phase on the SiO_2 dielectric, keeping the samples inside a dryer after the UV/O_3 cleaning.

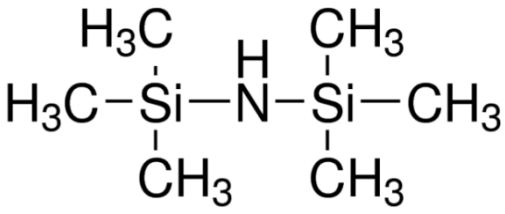


Figure 24: *Chemical structure of HMDS hexamethyldisilazane ($[(CH_3)_3Si]_2NH$).*

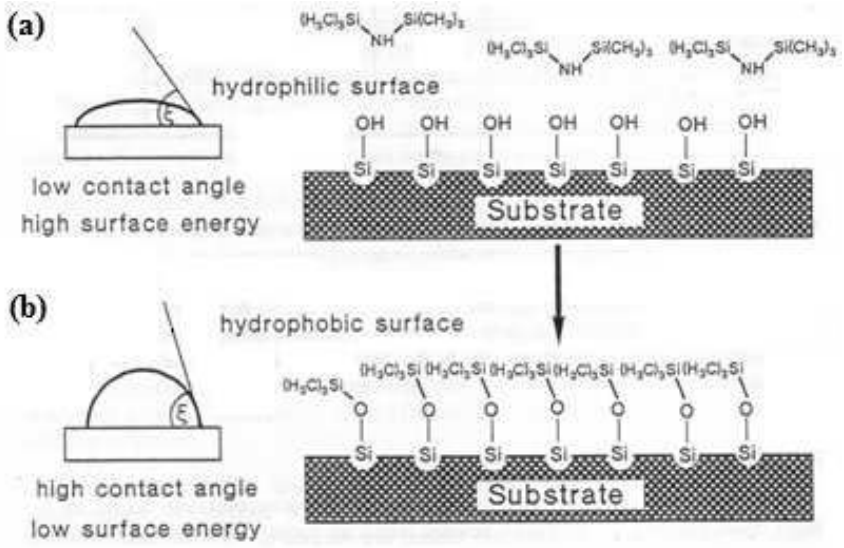


Figure 25: *Formation of the hydroxyl groups during the UV/O_3 treatment on a substrate, (b) alkane chains during HMDS process, and the respective contact angles.*

When the SiO_2 gate insulator is treated with UV/O_3, the insulator surface terminates with the hydroxyl groups, as shown in Figure 25(a). The hydroxyl groups make the gate insulator surface more hydrophilic, resulting in a mismatch of the surface energies between the gate insulator and the semiconductor film (Chou et al., 2006).To decrease the surface energy of the dielectric that was exposed to cleaning, and thus convert the hydrophilic gate insulator surface into a hydrophobic one, the HMDS coating is applied on the insulator, Figure 25(b). This monolayer consists on alkane chains $(CH_3)_3$) that modify the surface energy of the insulator and decrease the traps induced by the Si–OH groups on the gate dielectrics(Ohnuki et al., 2008).

The self-assembled monolayer is an insulating material, and charge conduction through the SAMs can be described by different theoretical models. The most common transport mechanism of alkyl SAMs is non resonant tunneling (Dibenedetto et al., 2009). The simplest tunneling model is assumed to be a direct tunneling, when it has a finite potential barrier Φ_B that can be overcome completely by the charges, or Fowler-Nordheim tunneling, when it is overcome partially (Beebe et al., 2006), (Aswal et al., 2006). These tunneling mechanisms depend on several factors, like applied voltage, type and thickness of the SAM, but they are independent by the temperature. Other possible SAM conduction mechanisms can be thermionic emission, Poole-Frenkel emission and hopping conduction(Aswal et al., 2006), (Dibenedetto et al., 2009). These models show a temperature dependence instead.

III.4.1. Temperature dependence of the SAM formation

By studies of Maboudian group, an intrinsic relation between the structure of the assembled alkylsilane and the deposition temperature is found (Carraro et al., 1998). According to Maboudian, during the SAM formation process on the silica, three different growth regimes and two characteristic temperatures, T_0 and T_c, exist. When temperature is below T_0, initially self-assembly process is formed only by island growth, while the area between the islands remains essentially unfilled. For temperatures between T_o and T_c, the growth of the islands is observed to occur more slowly than in the previous step, while the substrate regions between the islands are gradually filled in with the SAM molecules. For temperatures higher than T_c, no island nucleation is observed but the growth result homogeneous. In Figure 26 AFM images are shown of OTS grown at different temperatures: 10°C, 25 °C and 40 °C for a time of 30 s. At low temperature, it is possible to observe the developing of large islands. At room temperature, islands are much smaller compared to those present at low temperatures. While islands are not present at 40 °C.

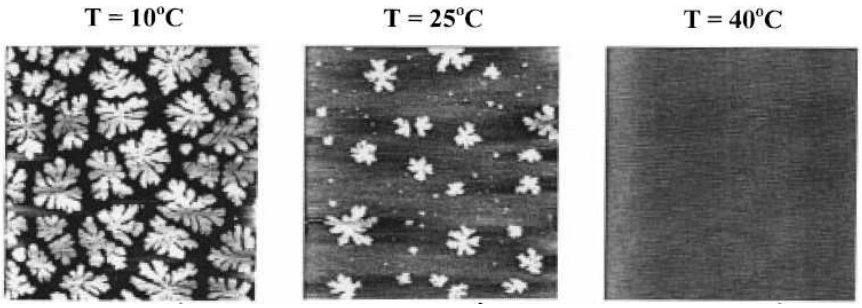


Figure 26: *AFM images of partial SAMs growth at temperature of 10 °C, 25 °C, and 40 °C.*

In Figure 27the histograms are shown of the profile distributions relating to the samples of Figure 26. It is been measured the depth below an arbitrary reference plane. For temperature of 10 °C and 25 °C, the distributions possess bimodal character, with two well-resolved Gaussian peaks. The peak at shallower depth is due to the islands. The separation between the two peaks indicates the average height difference, Δh, between islands and unfilled area. Δh takes name of the peak separation of the bimodal distribution. This difference is smaller for sample processed at 25 °C than for the ones processed at 10 °C, indicating larger material accretion between islands at higher temperatures. For temperature of 40 °C, the height distribution shows unimodal character.

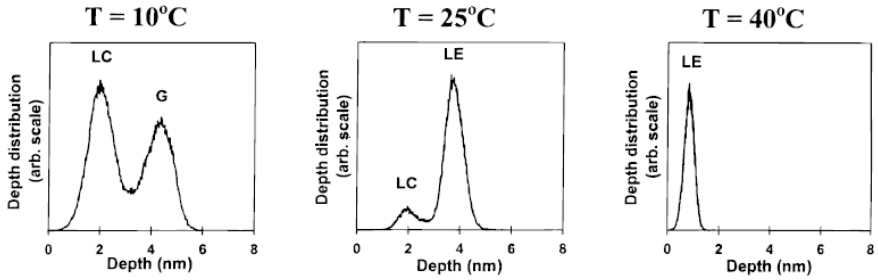


Figure 27: *Depth distribution histograms for the sample at temperature of 10 °C, 25 °C, and 40 °C.*

So, upon heating, the SAM formation process results homogeneous and without islands. Furthermore, another study claims that forming SAMs at temperatures above 25 °C can improve the kinetics of formation and reduce the number of the defects in them. (Kawasaki et al., 2000), (Yamada et al., 2000). Elevated temperatures increase the rate of desorption for adventitious materials and solvent molecules physisorbed on the surface of the substrate, and make it possible for the system to cross activation barriers for processes such as chain reorganization and lateral rearrangements of the adsorbates more easily than at room temperature. Yamada and co-workers suggest that the effect of the temperature is particularly relevant during the first few minutes of the formation of a SAM, when most of the adsorption and reorganization of the SAM is taking place.

III.4.2. Time dependence of the SAM formation

The SAM formation process is also sensible to the duration of the SAM process. An evidence is obtained from the observation of the time of evolution of the depth distribution as a function of the temperature (Carraro et al., 1998). The evolution of the peak separation, Δh, of the bimodal distribution is plotted in Figure 28 for different temperatures.

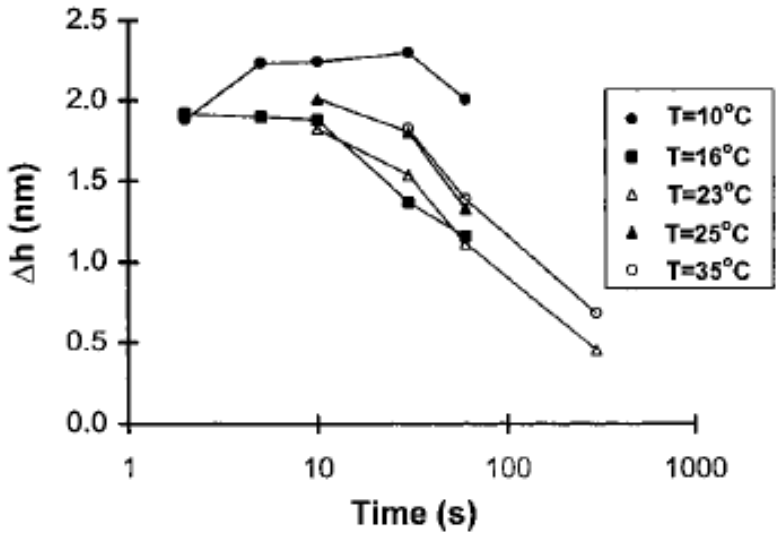


Figure 28: *Average peak separation distribution, Δh, as a function of the time for samples processed at different temperatures.*

At 10 °C, the peak separation remains approximately constant for as long as two peaks can be resolved, indicating that the exposed area between islands remains essentially free of SAM molecules. The growth pattern is remarkably different at higher temperature: the distance between islands and unfilled area peaks decreases with time, signifying that growth is occurring between islands. Anyway, island growth is observed to stop well before the island edges can touch. Finally, at temperatures of 40 °C and higher, growth occurs homogeneously, and no islands are detected: the depth profile distribution is now unimodal for all the immersion times.

III.5. Source and Drain Electrodes in OTFTs

The interface metal/semiconductor is an important aspect to improve the performances of OTFTs. A non-ohmic Schottky barrier can be formed at this interface and consequently the charge transport is limited. So, the choice of the contact metal is based on minimizing the height of the injection barrier that, for n-type OTFTs, is given by the difference between the metal Fermi level and the LUMO level of the organic semiconductor. In literature, fullerene n-channel transistors are reported prepared using a variety of high-workfunction and low-work function contact materials, such as gold (Haddon et al., 1995), (Horiuchi et al., 2002), (Kitamura et al., 2008), aluminum (Zhang &Kippelen, 2008), (Zhang et al., 2007), and calcium (Zhang & Kippelen, 2008). From these studies, it was observed no

systematic correlation between the choice of the metal and the C_{60} transistor performance for metals with workfunction ranging from 3 eV to 5eV. The relationship between the workfunction of the electrode and the contact performance may be related to a variety of phenomena occurring at the interface between the organic semiconductor and the metal, such as ‘‘pillow effect’’, namely the Coulomb repulsion between the electrons at the surfaces of the two materials, the presence of a thin oxide or a contamination layer, a large density of electronic gap states at the interface, or the presence of an interface dipole. Studies have found clear evidence that using calcium as contact metal provides better contact performance (Zhang & Kippelen, 2008), but n-type transistors show acceptable performance only if they are kept under vacuum or in an inert gas, otherwise the calcium reacts with oxygen and water vapor to form oxide and hydroxide.

So, for this thesis work, for the source and drain material the standard gold was chosen. Gold is historically the most studied material for this application, and it is an inert metal, that doesn't react with atmospheric gases and the chemicals most commonly used.

In the bottom contact configuration, the limitation of the performance of the device is given by the crystalline structure of the semiconductor at the electrode edge. From Dimitrakopoulos work (Dimitrakopoulos & Mascaro, 2001), it is demonstrated that a large number of grain boundaries are present at the edge of the Au contact with SiO_2 dielectric. In Figure 29 (a) it is shown a SEM image of a pentacene layer deposited on SiO_2 and on Au electrode without prior SAM deposition. In the top of the image, the grains size of the pentacene appears small on the Au, then passed the white area (Au), and far away from the Au edge, the dimension of the grains on SiO_2appears to larger size. So that, at the edge of the Au with the SiO_2 there is area region with small crystals and a large number of grain boundaries. Grain boundaries contain many morphological defects, that create charge carriers traps so inducing a reduction of the performances of the devices. In Figure 29 (b), it is illustrated the SEM image of a sample where the pentacene layer was deposited in the same way of the previous one, but the sample is pre-treated with a self-assembled monolayer (SAM) of 1-hexadecane thiol. Now, on both Au and SiO_2 large and similar grains sizes result. And there is no transition region at the Au edge. In this case, the mobility was three times larger than the mobility of the device with untreated surface. Traps were reduced by the SAM, that has modified the surface energy of the Au electrode, so improving the crystals (Dimitrakopoulos & Mascaro, 2001).

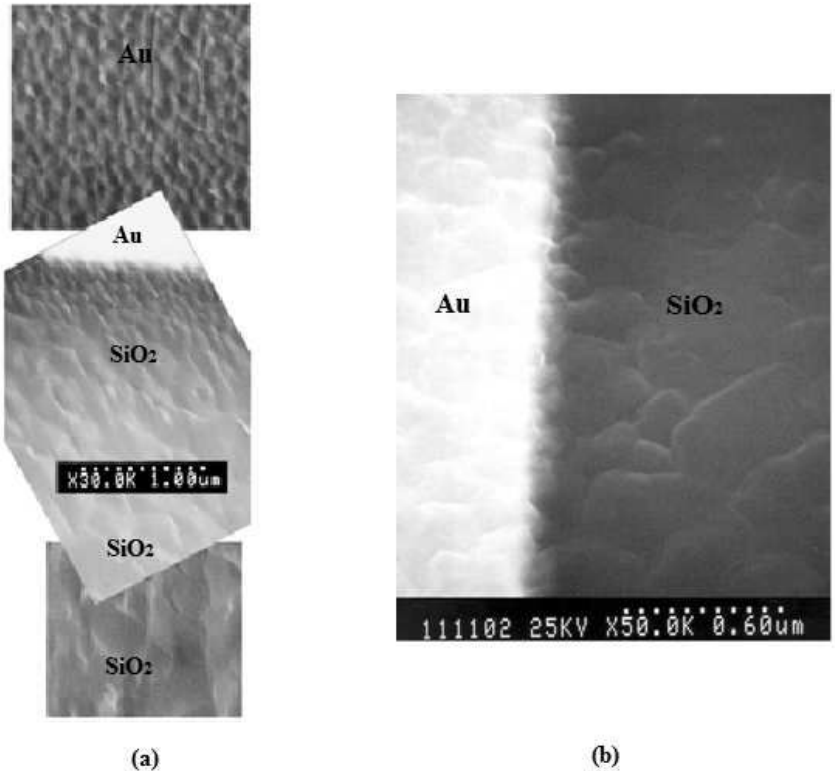


Figure 29: *SEM images of a pentacene thin film grown on SiO_2 and on Au electrode: untreated with SAM (a), treated with SAM of1-hexadecane thiol (b).*

III.6. Growth of Organic Semiconductor

In this thesis, the attention was focused on n-type organic semiconductors, and in particular on the [6,6]-phenyl-C71-butyric acid methyl ester ($PC_{70}BM$),a fullerene derivative used as the semiconductor in OTFTs(Chikamatsu et al., 2008), (Wobkenberg et al., 2008).

Figure 30 shows the molecule structures of fullerene C_{60}, Figure 30(a), and its derivate $PC_{70}BM$, Figure 30(b), respectively. $PC_{70}BM$ is soluble in various organic solvents as: chloroform, toluene, o-dichlorobenzene and xylenes, allowing an easy deposition from solution(Waldauf et al., 2003), and so being potentially much advantageous to integrate low-cost devices on large area and flexible substrates (Wobkenberg & Anthopoulos, 2008), (Anthopoulos et al., 2004), (Anthopoulos et al., 2005), (Yuan et al., 2014), (Myny et al., 2014), (Meyers et al., 2008), (Diao et al., 2013), (Yoo et al., 2014).This material can be processed in a variety of coating methods. Most of the literature refers to spin-coating method; however, other methods like

inkjet printing, spray coating, doctor blade and Meyer rods have attracted the interest of research groups(Diao et al., 2013), (Myny et al., 2014),(Meyers et al., 2008),(Yoo et al., 2014).

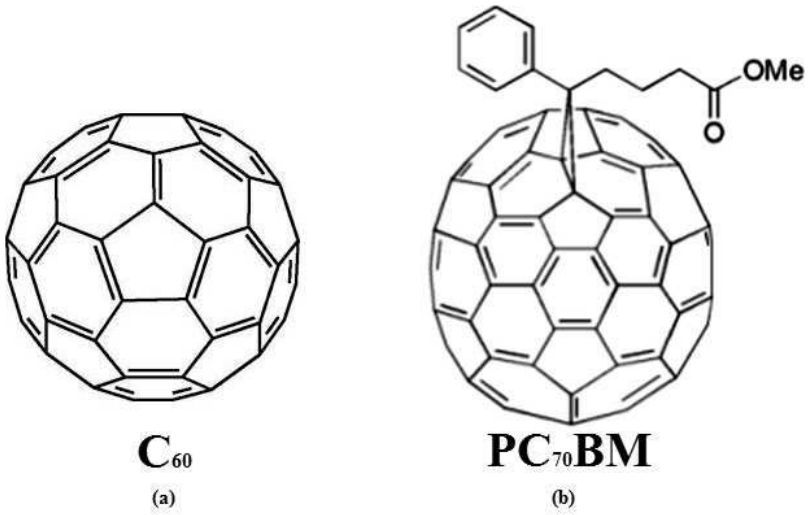


Figure 30: *Chemical structures of the fullerene C_{60} (a) and fullerene derivate $PC_{70}BM$ (b).*

However, this electron transporting material exhibits a low stability in air, and devices degrade rapidly and substantially upon air exposure. Stability of the n-type materials strongly depends on the free energy of activation associated with the chemical process/reaction with either water or oxygen. A possible solution for the air stability of negative charge carriers can be the formation of kinetic barriers that prevent diffusion of ambient oxidants into the active channel area (Katz et al., 2000), (Chikamatsu et al., 2008). Several research groups have reported the correlation between the crystallinity of fullerene films and their air stability (Ball et al., 2011). A way to overcome this problem is to use an efficient encapsulation of the OTFTs, to ensure long term stability.

In the state of the art devices that used fullerene derivatives, electron mobility and threshold voltage have reach values of :

$\mu = 0.1 \div 0.2$ cm²/Vs, $V_t = 7$ V,
structure: Glass/ITO/BCB/PC_{70}BM/Ca/Al
OSC deposition technique: spin coating (Wobkenberg et al., 2008)

$\mu = 4.6 \cdot 10^{-2}$ cm²/Vs, $V_t = 19.9$ V,
structure: Si/SiO_2/BCB/PC_{70}BM/Al
OSC deposition technique: spin coating (Rossbauer et al., 2014)

The electrical measurements in both cases were performed at room temperature under N_2.

In this thesis work, the drop casting technique was applied to deposit the $PC_{70}BM$. Drop casting is the easiest wet chemical method for the deposition of thin layers. It consists on the deposition of a drop of solution on a substrate. After that, the solvent can evaporate in a controlled environment leaving the solute on the substrate. This method presents some limitations, anyway, because it intrinsically produces inhomogeneous thin films, since during the solvent evaporation the solute tends to accumulate to the boundaries of the drop, due to the coffee-stain effect (Deegan et al., 1997), and it provides no major control with respect to the film thickness, that is proportional to the solution concentration. The advantage of this method is that the semiconductor can be deposited on a selected area on the sample, reducing the waste of material. Then, the solvent evaporation can be performed at the desired temperature. The heating of the substrate can speed up the solvent evaporation process and/or improve the film morphology.

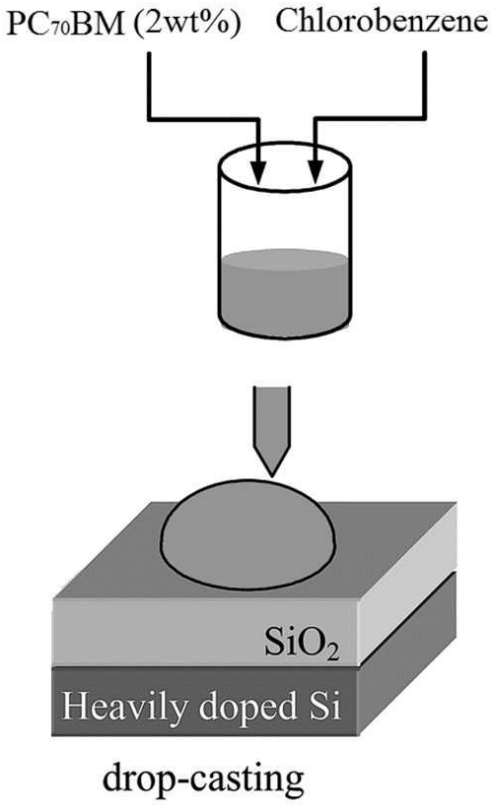


Figure 31: *Description of the drop casting technique process applied in this PhD work.*

In this thesis work, $PC_{70}BM$ powder was purchased from Solenne BV with a purity grade superior to 99%. The preparation of the thin films was done inside a glove box in inert atmosphere: the material was deposited by drop casting technique, Figure 31, from chlorobenzene solution (2 wt%) at room temperature, and afterwards all the samples were annealed on a hot plate at 60 °C for few minutes, to permit the solvent evaporation.

In the next chapter, the results of the characterizations of materials and devices are presented.

Chapter IV
Materials preparation and characterization and OTFTs DC analysis

In this chapter, the results of the fabrication steps and the analysis of the DC characterizations of the prepared transistors are reported. Contact angle measurements, atomic force microscopy (AFM), and DC and AC electrical measurements are the main characterization methods applied in this thesis. The objective is to study the effects of different treatments on the behavior of n-channel OTFTs for possible improvement of their performances, in term of charge carrier field-effect mobility, threshold voltage, and density of traps in the semiconductor. It is desirable to have the field-effect mobility as high as possible, because this significant parameter of the OTFTs determines the channel conductance and transconductance, as well as a small threshold voltage and a low density of traps. The AC measurements and their discussion are presented in the next chapter

IV.1. Analysis of HMDS Treatments

The variation of the OTFTs performances, due to the treatments of the dielectric/semiconductor interface, were firstly observed by studying the surface properties of the dielectric material.

A basic investigation, that monitor the quality of the SAM, was carried out using the water static contact angle (SCA), to ensure a reproducible fabrication process. Deviations of the SCA value can identify an error during the processing step of the SAM deposition. The SCA measurement is an effective technique to determine the wettability of self-assembled monolayers. A camera can be integrated to take photographs of the drop profile so as to measure the contact angle. The measurement is achieved by simply aligning the tangent of the sessile drop profile at the contact point

with the surface and reading the angle through the protractor in the eyepiece Figure 32.

The contact angle is the angle between the tangent to a drop's profile and the tangent to the surface at the intersection of the vapor, the liquid, and the solid phases. A low contact angle between a solid surface and a water-drop indicates that the surface is hydrophilic and has a high surface energy. On the contrary, a high contact angle means that the surface is hydrophobic and has a low surface energy. The contact angle of a liquid drop on an ideal solid surface is defined by the mechanical equilibrium of the drop under the action of three interfacial tensions:

$$\gamma_{lv}\cos(\theta_Y) = \gamma_{sv} - \gamma_{sl} \quad (25)$$

where γ_{lv}, γ_{sv}, and γ_{sl} represent the liquid-vapor, solid-vapor, and solid-liquid interfacial tensions, respectively, and θ_Y is the contact angle. The eq. (25) is usually referred to as Young's equation (Kwok & Neumann, n.d.), and θ_Y is Young's contact angle. Figure 32 shows an example of changing of how the surface wettability changes without and with a self-assembled monolayer. The SCA value depends on the chemical composition of the surface and is therefore specific for each SAM.

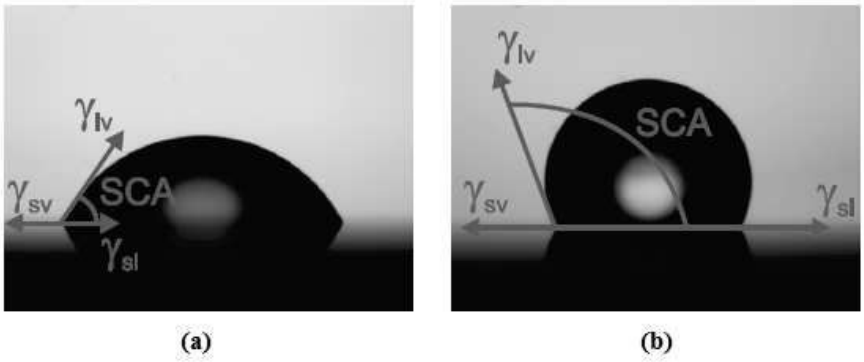


Figure 32:*Water drops on a sample surface, pre (a) and post (b) SAM deposition. The interfacial tensions and the resulting SCA are indicated in red color.*

IV.1.1. Results of the experimental step

In this thesis, the evaluation of the effect of the surface treatments was performed by static contact angle (CA) measurements of H_2O, using a contact angle system Dataphysics OCA20, Figure 33, in sessile drop mode with a drop volume of 0.5 µL. The surface treatments of the SiO_2 gate insulator and the corresponding contact angle values are shown in Table 1.

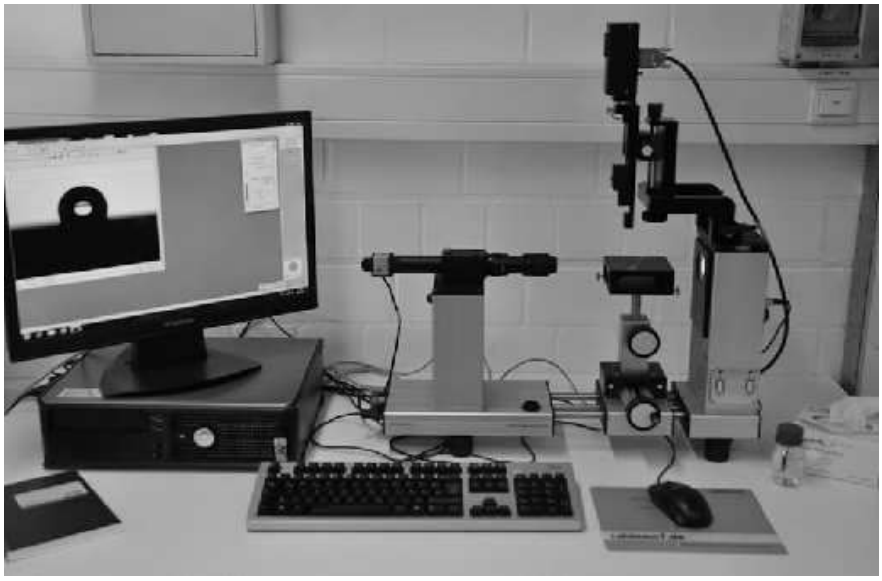


Figure 33:*Contact angle system Dataphysics OCA20 present at the ENEA Research Centre in Portici.*

As shown in Table 1, UV/O_3-only treated samples showed lower contact angle values than untreated samples. When SiO_2 gate insulator is cleaned with UV/O_3 process, unstable dangling bonds of hydroxyl groups can make the SiO_2 surface more hydrophilic; this means to have highly polar surfaces. Residual organics on the terminals of the hydroxyl groups can form on the insulator surface (Park et al., 2002). The contact angle is expected to decrease as the quantity of organic residues is reduced. In general, hydrophilic state of the inorganic oxide surfaces and hydrophobic state of the organic semiconductors create a mismatch that can influence negatively the deposition of the semiconductor layer on an oxide substrate. HMDS treatment can improve the quality of the growth of an organic semiconductor, in terms of the material crystallinity and so for the charge carrier mobility (Ulman, 1991). So, the samples treated with HMDS showed a large increase of the contact angle value, confirming a more hydrophobic character of the surface was obtained. The images of the contact angles, reported in Figure 34, show the variation of the CA values after each treatment.

Table 1: *Summary of the surface treatment conditions and SiO_2 contact angle values.*

Substrate	UV/O_3	HMDS deposition temperature	SiO_2 contact angle
$Si/SiO_2/Au$	Untreated	Untreated	30.6°±0.5°
$Si/SiO_2/Au$	20 min	Untreated	3.5°±0.1°
$Si/SiO_2/Au$	20 min	7°C	106.1°±0.3°
$Si/SiO_2/Au$	20 min	25°C	109.3°±1.0°
$Si/SiO_2/Au$	20 min	60°C	104.1°±0.5°

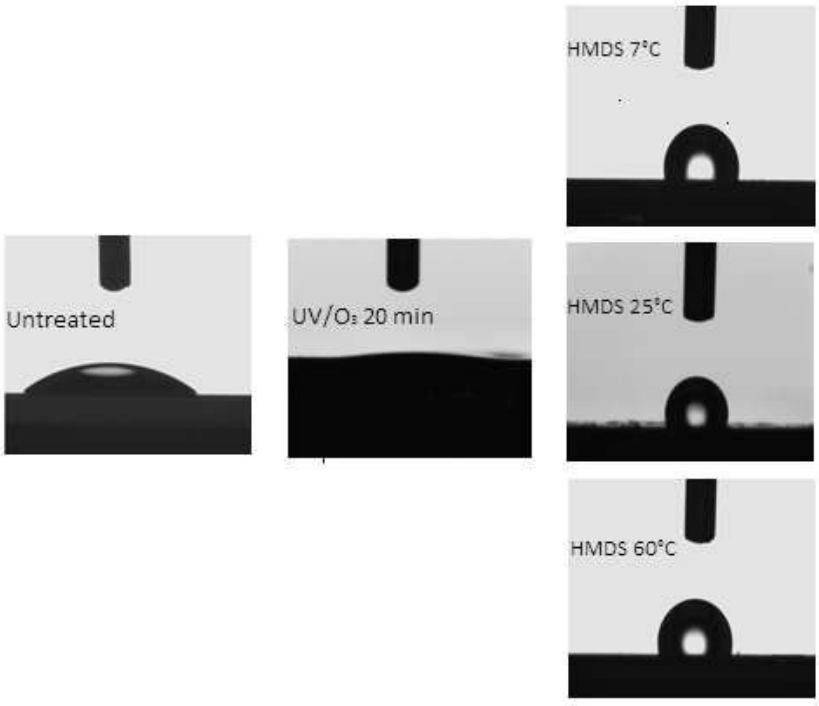


Figure 34:*Contact angle images for SiO_2 substrates treated at different HMDS deposition temperatures*.

The uncertainty of the CA measurements is calculated as the average value on 20 samples for each typology.

As it is possible to observe from Table 1 and Figure 34, the different deposition temperatures of the SAM (7°C, 25°C, 60°C) allowed to obtain surfaces with different hydrophobicity. This is probably due to a different

condensation behaviour of the HMDS, that varies with the temperature (Carraro et al., 1998).

IV.2. Morphology Analysis of the deposited Organic Semiconductor

To investigate the effect of the surface conditioning on the semiconductor, the atomic force microscopy (AFM) was used. AFM measurements can provide a direct image of the surface morphology of the material and allow the detection of defects at nanometer scale. In Figure 35 Figure 35 it is shown the basic working principle of an AFM. It employs a cantilever, made of silicon or silicon nitride, with a sharp tip of pyramid shape, to scan the sample surface. The deflection or oscillation amplitude of the cantilever is acquired by bouncing a laser beam off of it and into a position-sensitive detector. Detected movements in cantilever are corrected to a set-point value by actuating the cantilever via a feedback-controlled piezo. The corrected signal is then converted into a high resolution topographical map of the surface. The AFM offers two modes to investigate a surface: contact mode and tapping mode. In contact mode, the tip physically touches the surface of interest. In tapping mode, instead, the tip is not dragged over the surface but it oscillates up and down near its resonance frequency (Geisse, 2009) over the sample surface. So tapping mode is most suitable for soft polymeric surfaces that could be easily damaged by a touching tip. Special techniques related to AFM are capable to measure several surface properties such as elasticity, friction or the surface potential (Ellison et al., 2011), (Kuna, 2009).

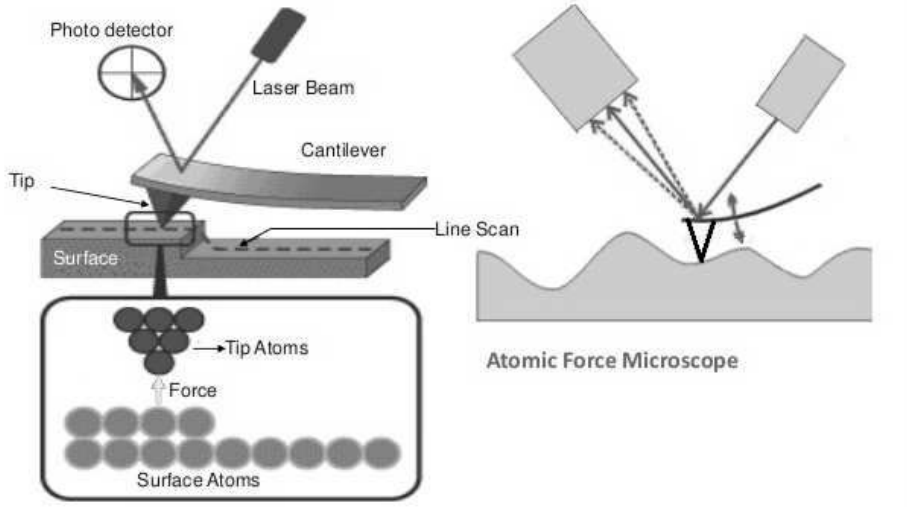


Figure 35:*Shematic diagram of the working principle of AFM.*

IV.2.1. Results of the experimental step

To evaluate the $PC_{70}BM$surface roughness, an AFM Veeco NSIV model was used in tapping mode. In Figure 36 the images of the semiconductor films deposited on the transistors channel area are shown for the three types of HMDS deposition temperatures. The different hydrophobicity of the SiO_2 surface leads to obtain $PC_{70}BM$ thin films characterized by very different roughness, as reported in Table 2.

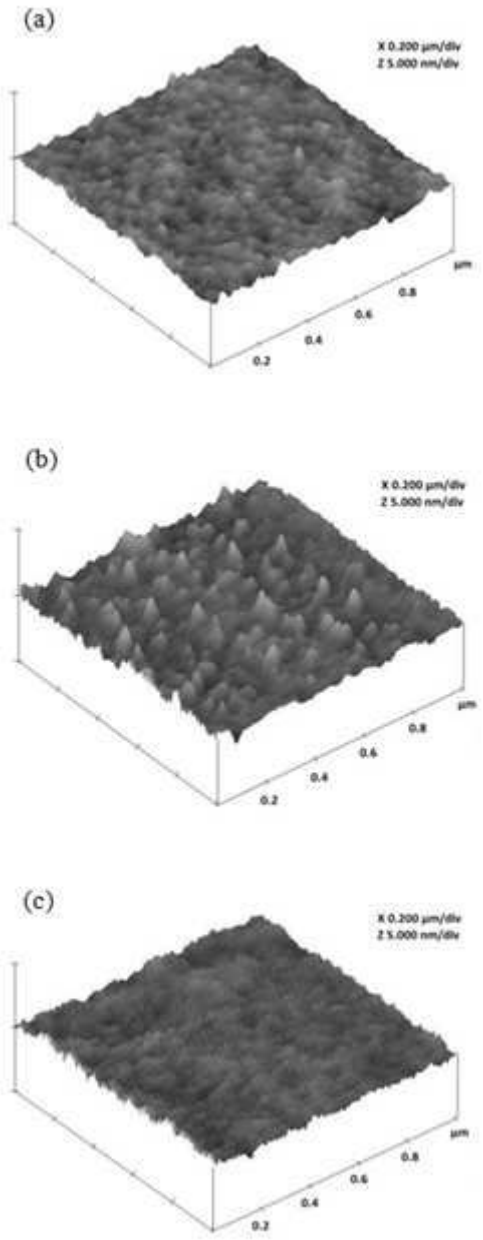


Figure 36: *AFM images of $PC_{70}BM$ thin films deposited on SiO_2 dielectric treated with HMDS: (a) at 7°C; (b) at 25°C; (c) at 60°C.*

The $PC_{70}BM$ films obtained on HMDS deposited at 7°C and 60°C, show the most homogeneous surface, whereas the HMDS obtained at 25°C induces the formation of a very inhomogeneous surface with high roughness.

The condensation mechanism of the HMDS varies with the preparation conditions, in particular with the deposition temperature, its action reveals more efficient during the processes at 7°C and 60°C. Indeed, the reduced surface energy (i.e., highest contact angle) for the samples obtained at 25°C, leads to increase of the number of nucleation sites, which results in a great variation of the grain sizes and therefore an increase of the surface roughness (Chang et al., 2003), (Sze, 1985).

Table 2*: Roughness and grain mean size measurements of the $PC_{70}BM$ films at the various SiO_2 surface treatment conditions.*

Devices	Roughness rms (nm)	Grain mean size (nm)
UV/O_3 20 min + HMDS 7°C	0.17 ± 0.01	25 ± 2
UV/O_3 20 min + HMDS 25°C	0.30 ± 0.07	40 ± 10
UV/O_3 20 min + HMDS 60°C	0.18 ± 0.02	25 ± 3

IV.3. DC Measurement

The fabricated OTFTs were electrically characterized using a probe station CASCADE Summit 11000B-M at room temperature, keeping each sample under nitrogen flow during all the measurements, to avoid the perturbing influence of the water on the measurements (Jung et al., 2005). The data acquisition was done using a Keithley 4200-SCS Semiconductor Characterization System. The source and drain pads, which are accessible from above the samples, were connected through two thin needles moved by precise positioning manipulators, while a conductive sample holder was used to connect the bottom gate contact.

The DC characteristics of the OTFTs were analyzed to extract some fundamental electrical parameters according to the classical MOSFET equation for the saturation regime (Sze, 1985):

$$I_{DS} = \frac{W\ C_i}{2L}\mu_{SAT}(V_{GS} - V_T)^2 \qquad (26)$$

where W and L are the width and the length of the channel, respectively, C_i is the insulator capacitance per unit area, V_{GS} and V_{DS} are the voltages at gate and drain electrodes related to the source potential, V_T is the threshold voltage, μ_{SAT} is the field effect mobility in saturation. The threshold voltage was estimated from the curve $\sqrt{I_{DS}}$ *vs.* V_{GS} by means of the intercept method, while the charge carrier mobility is determined from the same curve in saturation regime by extrapolation at the same V_{DS} polarization.

IV.3.1. Results of the experimental step

The devices fabricated without the SiO_2 surface treatments (one or both) are not presented, because no meaningful data were obtained during measurements.

The channel current I_{DS} was measured varying the V_{GS} and V_{DS} values from 0 V to 60 V. In Figure 37, Figure 38, Figure 39 are shown the electrical results belonging to the most representative samples for each of the three different deposition temperatures, while in Figure 40 it is illustrated the comparison of their output (a) and transfer curves (b) at fixed V_{GS} and V_{DS}, respectively.

In Table 3, mobility and threshold voltages extracted from the I-V transfer curves are summarized for each treatment condition.

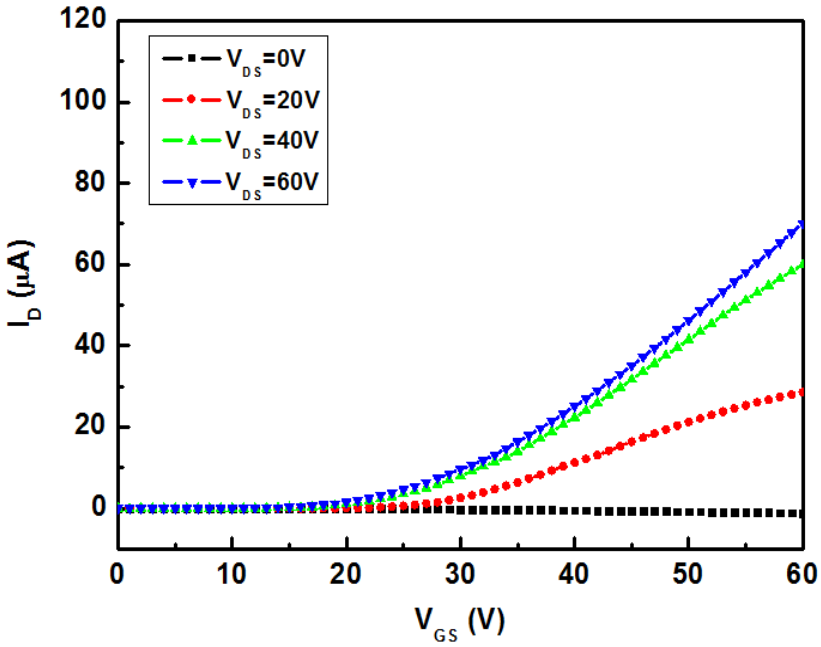


Figure 37:*Transfer curves of $PC_{70}BM$ based OTFTs obtained for HMDS deposition at temperature of 7°C.*

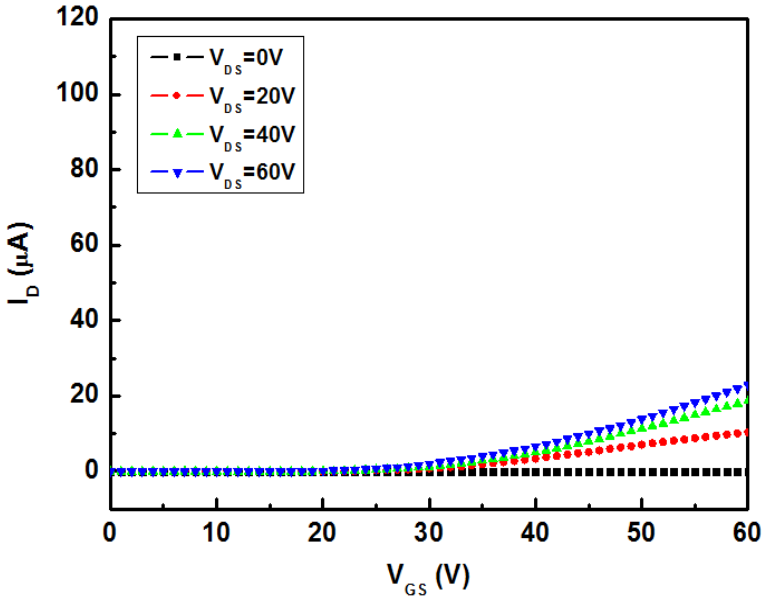


Figure 38:*Transfer curves of $PC_{70}BM$ based OTFTs obtained for HMDS deposition at temperature of 25°C.*

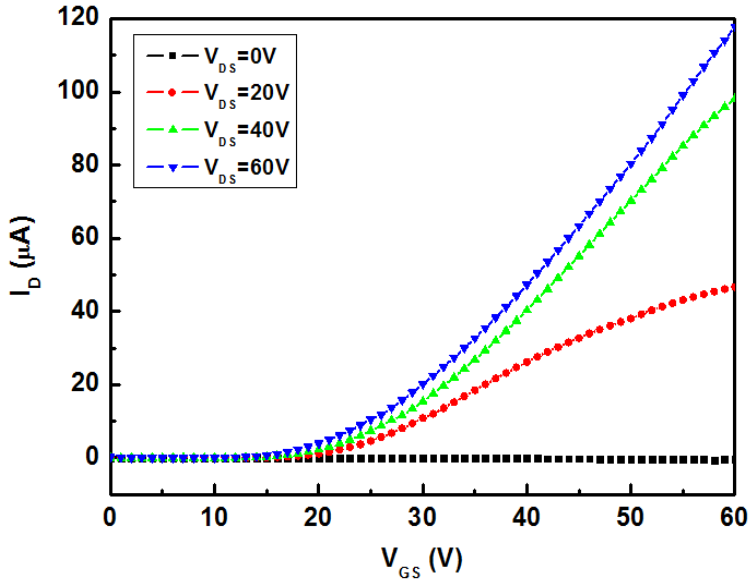


Figure 39:*Transfer curves (b) of $PC_{70}BM$ based OTFTs obtained for HMDS deposition at temperature of 60°C.*

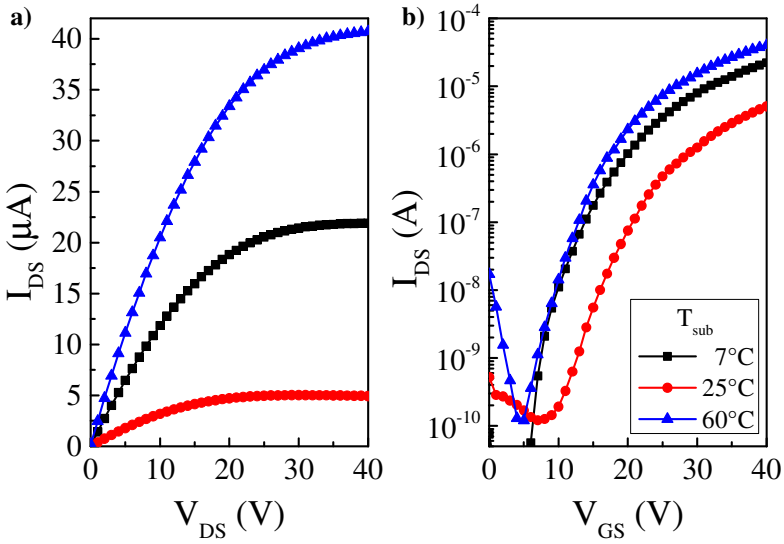


Figure 40: *Comparison of the output (a) and the transfer (b) curves for the OTFTs prepared using the HMDS deposited at the three different temperatures; the two types of curves were respectively measured at V_{GS} = 40V and V_{DS} = 40 V.*

Table 3*: Electrical parameters of the OTFTs for the different HMDS deposition temperatures (mean values and errors from 20 samples).*

Devices	μ_{SAT}(cm^2/Vs)	V_T(V)
UV/O_3 20 min + HMDS 7°C	7.64±0.06 10^{-3}	13.69±0.07
UV/O_3 20 min + HMDS 25°C	2.88±0.02 10^{-3}	17.80±0.05
UV/O_3 20 min + HMDS 60°C	1.30±0.01 10^{-2}	12.01±0.05

From the extracted values it is possible to observe that the samples prepared with HMDS deposited at 60 °C exhibit the highest electron mobility, $13 \cdot 10^{-3}$ cm^2/Vs and the lowest threshold voltage, 12.0 V. Conversely, the devices obtained at 25°C show the lowest mobility, $2.8 \cdot 10^{-3}$ cm^2/Vs, and the highest threshold voltage, 17.8 V. Samples fabricated at the HMDS deposition temperature of 7 °C display intermediate performance, but closer to the 60 °C devices.

IV.4. Discussion of the data - Comparing the electrical parameters vs. the hydrophobic characteristics

To evaluate the performance of the fabricated OTFTs, the electrical parameters are put in relationship with the contact angle measurements. In particular, in Figure 41, the field effect mobility and the threshold voltage of the OTFTs (from Table 3) are plotted versus the contact angle values of the respective substrate as reported in Table 1.

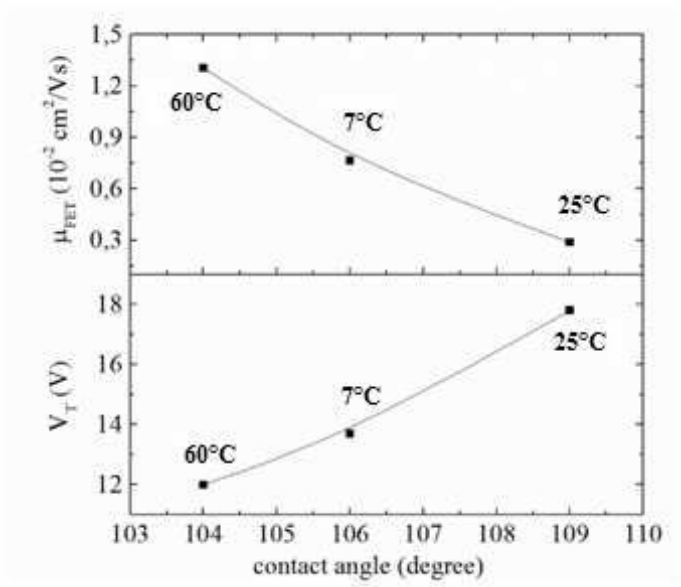


Figure 41: *Field effect mobility and threshold voltage of the fabricated OTFTs vs. the contact angle of the substrate surface.*

For the used materials, the results show that the greater hydrophobicity do not imply the best mobility. The highest values of the contact angle are for the HMDS deposition at 25°C temperature, while mobility here presents the lowest value. As seen before, this higher hydrophobicity of the SAM induces the formation of very rough films of $PC_{70}BM$, which can be due to inhomogeneous dimensions of the crystalline grains, as indicated by the AFM analysis from Table 2, so giving the smaller value of the mobility because of the scattering of the charges along the devices channel. The samples for HMDS deposition at temperature 60°C show the best OTFTs performances. This temperature allows the formation on the gate dielectric of a SAM whose surface energy is best matched with the $PC_{70}BM$

semiconductor, so more homogeneous films are obtained and therefore a higher charge carrier mobility can result. Lastly, the samples at 7°C give intermediate results, both in terms of OTFTs performance and of hydrophobicity. So, for bottom-gate devices, it can be concluded that, to obtain a good growth of an organic semiconductor and a tailored interface with the gate dielectric, it is necessary to develop and apply specific treatments of the underlying surface, that induce a specific level of hydrophobicity.

Chapter V
Equivalent Circuit AC Model

Over the last decade, much effort has been done on the investigation and modeling of the electrical properties of the OTFTs (Necliudov et al., 2000), (Oberhoff et al., 2007), (Torricelli et al., 2008). However, literature on AC characterizations of transistors that employ electron transporting semiconductors is limited, while organic p-type semiconductors have been intensively studied (Kim & Kim, 2010), (Zaki et al., 2014), (Zaki et al., 2013). In this chapter, the attention is focused on the AC characterization of the fabricated OTFTs and on the study of an equivalent circuit model that for the first time, is developed to interpret the experimental data of a n-type OTFT in a bottom-gate bottom-contact (BGBC) geometry. As already said in Chapter II, this configuration is very convenient for the design of the circuit wiring, because it can be prepared before the deposition of the semiconductor, so without affecting this one with aggressive processes.

It is well known for the metal-oxide-semiconductor devices based on crystalline, polycrystalline, and amorphous silicon that the presence of trapping states located at the interface semiconductor-insulator and in the bulk of the materials can cause instabilities in the threshold voltage value. Admittance measurements was proved particularly useful for studying such states in silicon devices (Nicollian & Goetzberger, 1967). These measurements are used also to give an insight into the device physics of organic thin film transistors.

In this chapter, it has been performed the analysis of the admittance measurements, supported by Nicollian (Nicollian & Brews, 2002), to reveal some interesting parameters, such as the density of states for the electron traps present in the semiconductor and at the interface between $PC_{70}BM$ and silicon oxide. The parameters are not measured directly by admittance measurements, but they can be extracted from measured admittance using an equivalent circuit.

An accurate modeling of the dynamic response of the OTFTs is proposed to interpret the observed differences of the admittance curves and determine the devices features induced by the deposition processes in the three cases

under analysis. The proposed model reveals the critical role played on the devices performance by the quality of the insulator-semiconductor interface and by the growth of the semiconductor, which can be enhanced by suitable treatments. The model is also used to define the relationship between the contact angle of the substrate and the quality of both the semiconductor at the interface with the insulator and the semiconductor bulk; this quality has been described using the localized state density.

This analysis wants to investigate the existence of a peculiar level of surface hydrophobicity, obtained from a combination of temperature and time of the HMDS deposition, to obtain good OTFTs performance.

V.1. AC Measurement

After the static characterizations of the previous chapter, the relationship between the properties of the deposited semiconductor films and the electrical characteristics of the transistors have been evaluated also through admittance measurements.

A metal-insulator-semiconductor (MIS) capacitor structure allows the use of small-signal impedance techniques to study the interfacial states. Gundlach has recently introduced the possibility of performing admittance measurements on particular configurations of TFTs, i.e. the ones with a BC structure (Hamadani et al., 2008). Let's here describe the spectroscopy measurement technique that is used for the BGBC configuration of a transistor.

For the organic transistors, the impedance spectroscopy is carried out by shorting together the drain and source electrodes and applying, between them and the gate electrode, an AC small amplitude signal (V_{ac}~10 mV) at variable frequency and a DC bias range, as shown in Figure 42.

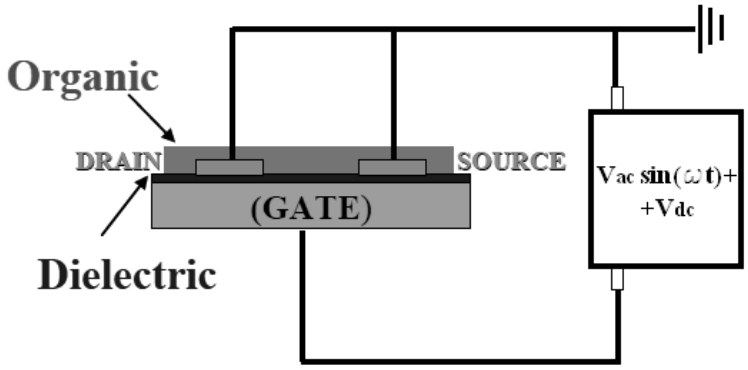


Figure 42: *Schematic diagram of the characterization set-up for the AC measurements of BC OTFTs.*

The measurements are performed using a LCR meter: it provides the input signal and measures the device capacitance and conductance as a function of a DC gate bias and frequency. The capacitance gives information about the polarization properties and of all the carriers that are able to follow instantaneously the electric field, included defects and impurities. The measure of the conductance divided by the angular frequency (this ratio is named "loss") takes into account of the energy dissipated by the device.

Furthermore, by varying the DC gate bias, it is possible to monitor the dynamics of the charge carriers accumulation in the channel of the transistor. In response to the AC gate voltage, the majority carriers flow in and out of the depletion layer: this leads to a capacitance behavior in accumulation and in depletion respectively. Majority carrier charges follow the AC signal as long as the period of the AC voltage is much longer than the dielectric relaxation time of the semiconductor τ_D, which is equal to the product of the resistivity and the permittivity of the organic material. In other words, majority carriers respond when $1/\omega >> \tau_D$, where ω is the angular frequency of the AC voltage. At room temperature, minority carrier response is much slower than that of the majority carriers; it is governed by the bulk traps having energy levels in the semiconductor bandgap near midgap and spatially distributed throughout the organic depletion layer. For this reason, minority carriers are considered negligible (Hamadani et al., 2008).

V.1.1. Results of the experimental step

The properties of the semiconductor films of the samples obtained at the HMDS deposition temperatures 7 °C, 25 °C and 60 °C, and durations 4 days, 1day and 1 day, respectively, are investigated through admittance measurements. The measurements were done maintaining the devices in a cryostat at a pressure of $7 \cdot 10^{-5}$ mbar at room temperature. The capacitance and the conductance data were collected with a LCR meter Agilent E4980, using the configuration in Figure 42. The used frequency ranged from 20 Hz to 2 MHz and the DC bias between -40 V and 40 V. Different bias is used to pass from the depletion regime to accumulation regime.

Before doing the AC measurement, two compensations are necessary: open and short compensation. These steps reduce the effect of the residual series impedance and parallel admittance, respectively, due to the connections and the error introduced by the contact resistances.

Admittance $Y(\omega)$ was measured as a function of both bias and frequency, according to the parallel model $Y(\omega)=G_P(\omega)+j\omega C_P(\omega)$, where $G_P(\omega)$ and $C_P(\omega)$ are respectively the conductance and the capacitance as a function of the angular frequency.

The first step in the analysis on how the surface treatment affects the material properties and thus the device performances was carried out by measuring the frequency response of the admittance. Examples of the

admittance characteristics of the fabricated transistors for each typology are reported in Figure 43, Figure 44 and Figure 45, for the samples realized at 7°C, 25°C and 60°C, respectively. 20 devices were tested for each category.

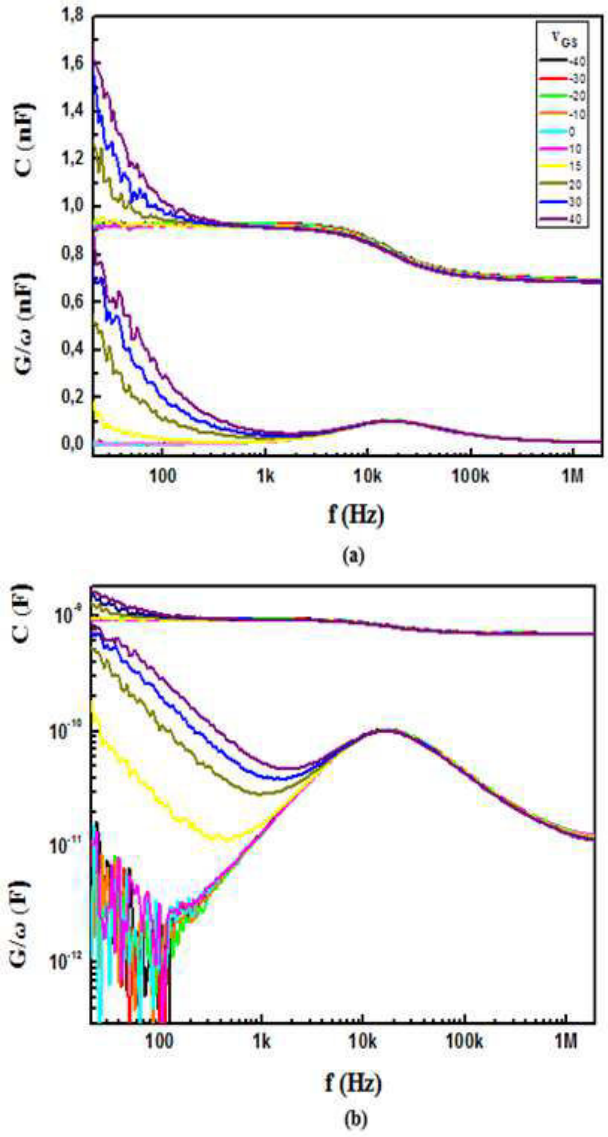


Figure 43: *Representative capacitance and loss curves for samples at 7°C measured at various biases as a function of the signal frequency, (a) in linear scale and (b) in logarithmic scale.*

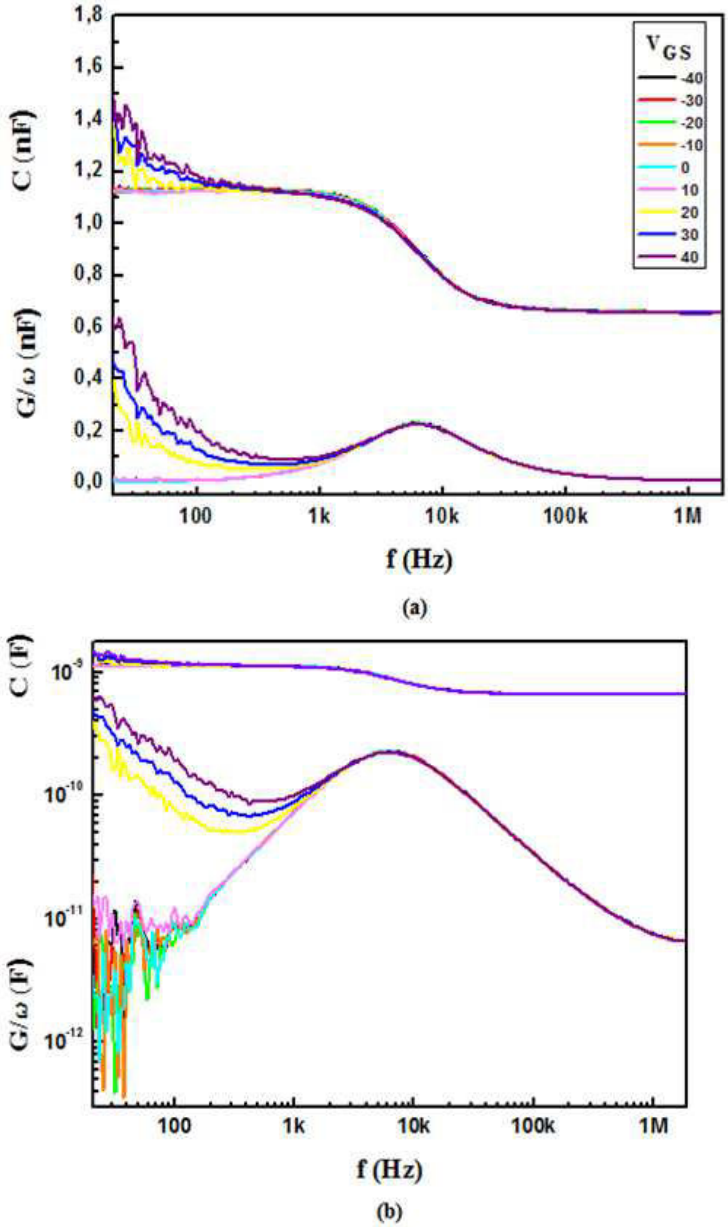


Figure 44: *Representative capacitance and loss curves for samples at 25°C measured at various biases as a function of the signal frequency, (a) in linear scale and (b) in logarithmic scale.*

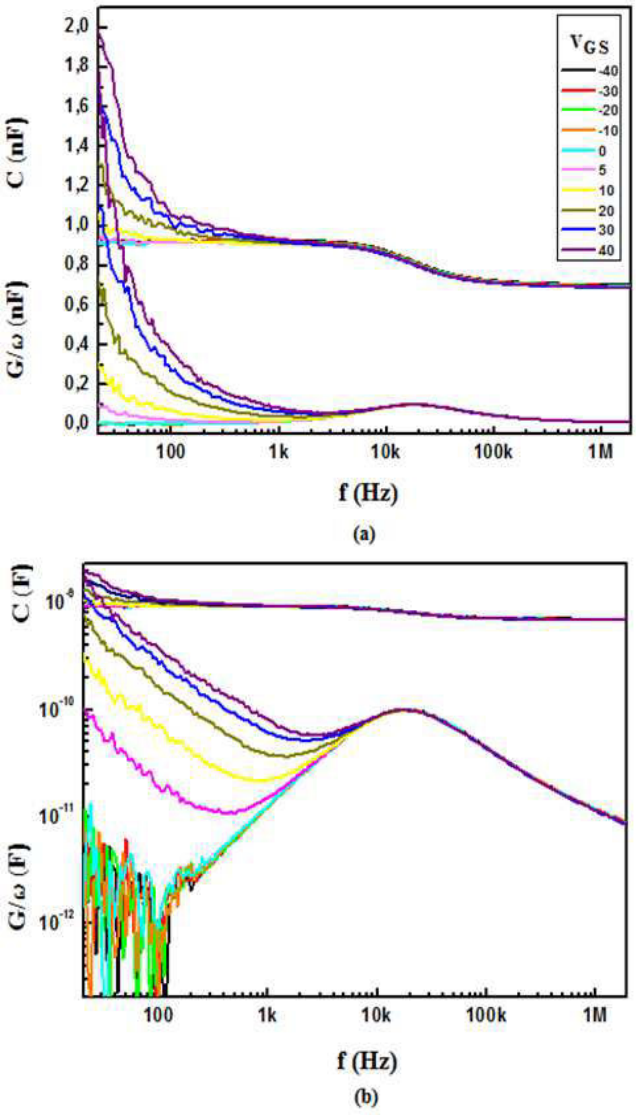


Figure 45: *Representative capacitance and loss curves for samples at 60°C measured at various biases as a function of the signal frequency, (a) in linear scale and (b) in logarithmic scale.*

The liner plots in the figures (a) focus the attention on the capacitance variation, while the logarithmic plots in (b) brings out the presence of the dispersion peaks. It is possible to observe that at the low frequencies, up to about 1 kHz, a strong bias dependence is evident: both capacitance and loss increase with the gate bias above the threshold voltage, in accordance also with the C-V curves shown in Figure 46. In particular, the capacitance increases when the devices are driven from depletion regime, where the

capacitance is at the lowest value, defined as the device geometric capacitance, and it is equal to the series of the insulator and depletion layer capacitances, towards accumulation regime, where C_p achieves its highest values. In accumulation regime, the capacitance corresponds to the insulator capacitance. On the contrary, the dispersive phenomenon that appears at intermediate frequencies weakly depends on the bias and can be ascribed to the presence of traps in the semiconductor. In particular, the structural disorder of the organic semiconductor imposes an upper limit on the frequency, after which the injected electrons are not able to follow the applied AC signal. Furthermore, at very high frequencies, it can be detected a tail of the dispersion, visible in the loss curves, that can be attributed to a small series resistance due to the electrodes (Nicollian & Brews, 2002).

The second step of the analysis was dedicated to the measurements of the capacitance as a function of gate voltage. The collected data are presented in Figure 46.

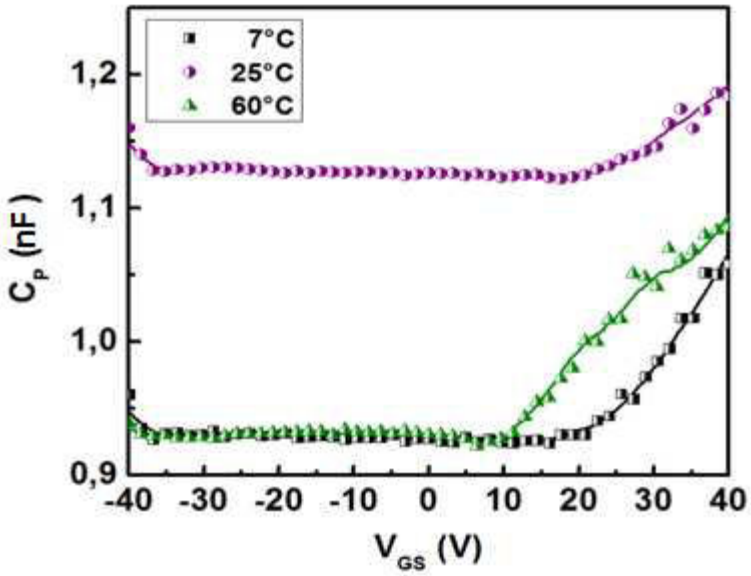


Figure 46: *Capacitance measured as a function of the gate voltage at the fixed frequency of 100 Hz for samples at 7°C, 25°C and 60°C.*

In Figure 46, all the curves show an increase of the capacitance starting roughly close to the threshold voltages extracted from the I-V curves, which may indicate the transition from the depletion to the accumulation regime at high positive voltages.

An evident difference in the curves is in the higher depletion capacitance level of the sample processed at the HMDS deposition temperature of 25°C, equal to 1.13 nF, different by 0.93 nF of the cases of the samples fabricated at the HMDS deposition temperature of 7°C and 60°C. The cause could be

associated to a different trap state density in the semiconductor. Indeed, the Figure 47 shows the comparison of the admittance curves as a function of the frequency for the three types of OTFTs in the region of accumulation at V_{GS}= 40 V. By observing the obtained data, it is seen that the samples at HMDS treatment temperatures of 7°C and 60°C have a similar trend at the intermediate frequency, while the dispersion in the device at 25°C results to be much higher and shifted in frequency. This factor of difference probably indicates a higher concentration of defects (Nicollian & Brews, 2002). A further difference in the curves is found at high frequency, for treated samples at 7°C and 25°C, respect the sample at 60°C: it is visible the tail of a third dispersion peak which is introduced by a contact series resistance (R_C) (Nicollian & Brews, 2002) which is of the order of a few tens of ohm.

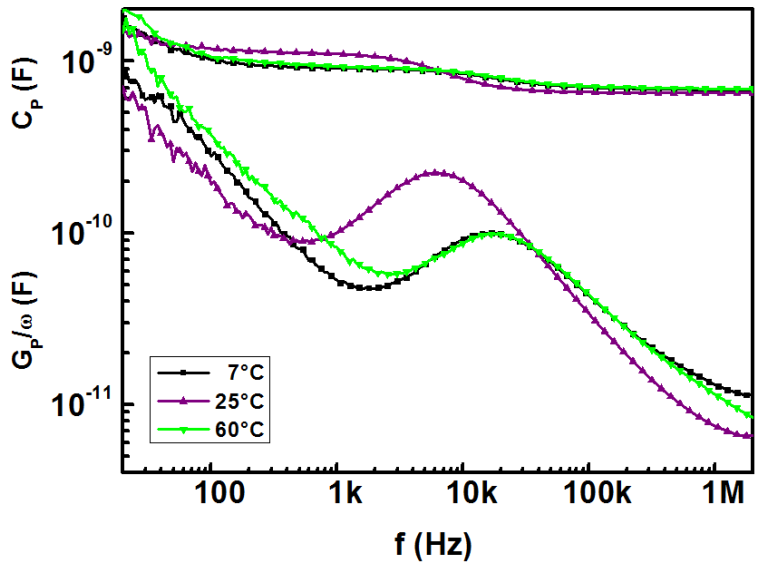


Figure 47: *Capacitance and loss measured as a function of the frequency at the fixed gate voltage of 40 V for samples at 7°C, 25°C and 60°C.*

V.2. Interface Characterization Technique

To obtain information on the traps and their properties present in the organic semiconductor, it is necessary to extract the corresponding parameters from the measured admittance using an equivalent circuit. So, an equivalent circuit is here presented to determine the devices features in the three cases under analysis.

The physics behind the admittance measurement is based on capture and emission of mobile carriers by the trap levels distributed throughout the OSC bandgap. There are many methods for measuring the electrical properties of

the traps. Some examples are: transient methods emission time spectroscopy (Shulz & Jonson, 1977), thermal dielectric relaxation current (Simmons & S., 1974) and optical methods (Kamieniecki & Niticki, 1978), (Dahlke & Greve, 1979). However, the small-signal steady-state method is the most widely used (Nicollian & Brews, 2002).

The trap states are located at the OSC-SiO_2 interface and in the semiconductor bulk. These defects can interact with the orbital of the semiconductor molecules to capture or emit electrons by varying the gate bias, that is traps can exchange charges with the OSC.

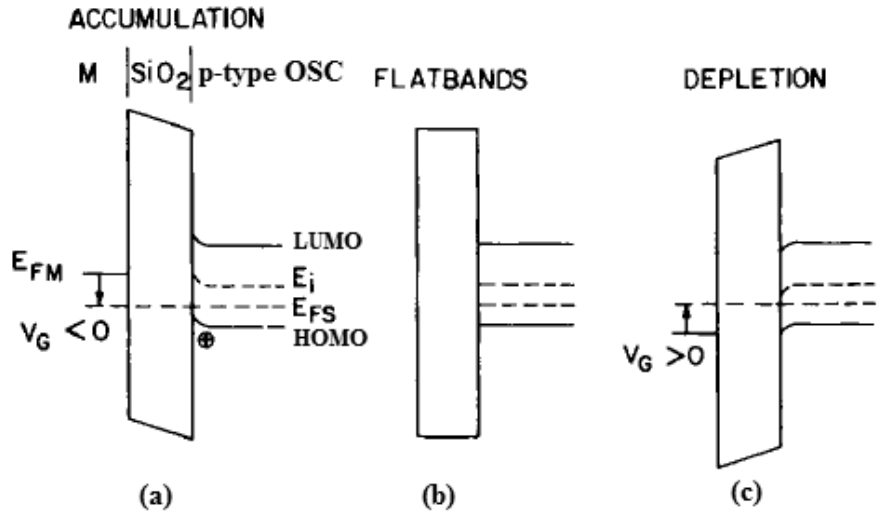


Figure 48: *Band-bending diagrams as a function of the applied gate bias, considering a device with OSC of p-type: (a) accumulation regime (negative gate bias), (b) flat-band (no gate bias), (c) depletion regime (positive gate bias). HOMO e LUMO are highest occupied molecular orbital and lowest unoccupied molecular orbital, respectively; E_i is the intrinsic Fermi level; E_{FS} is the Fermi level in the OSC; E_{FM} is the Fermi level in the metal (Nicollian & Brews, 2002).*

In the accumulation regime (Figure 48 a), when a very large negative gate bias is applied, the HOMO band edge bends up towards the Fermi level. In this case, the interface trap levels are empty by capturing majority carriers until the equilibrium condition is reached. At a very large negative bias, hole density at the OSC surface exceed hole density in the bulk. As gate bias is reduced to zero (Figure 48 b), the bands appear flat. Trap levels below Fermi level are full of charge carriers, while those above are empty. As a positive gate bias is applied (Figure 48 c), the LUMO band edge bends down towards the Fermi level and the trap levels fill by charge carriers until the equilibrium

conditions. Furthermore, holes are repelled from the OSC surface and consequently occurs the formation of the depletion layer.

If a small AC voltage is applied to the gate of the OTFTs, it alternately moves the band edges towards or away from the Fermi level, producing the capture and the emission of the majority carriers. So that, charge carriers change occupancy of the trap levels in a small energy interval centered about Fermi level. Capture and emission of the carriers cause an energy loss, that is measured as an equivalent parallel conductance G_P, divided by the angular frequency ω. Furthermore, the traps can hold charge carriers for some time after the capture, for this reason traps store charge and it is possible to calculate trap level density as proportional to a capacitance, C_t.

V.3. Equivalent electrical model

In this thesis, the properties of the semiconductor bulk and the conductive channel are estimated in relation to the substrate quality. To effectively describe the AC behavior of the devices, a lumped electrical equivalent circuit is proposed, with parameters dependent on the operational regime and on the fabrication routes. The general equivalent circuit is derived from various theoretical considerations and experimental observations. In particular, the OTFT configuration used has source and drain shorted together and the OTFT is modeled as an RC network. In Figure 49 the proposed electrical model is shown.

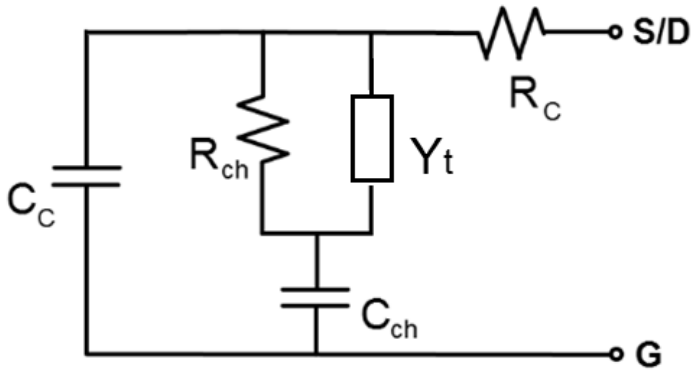


Figure 49: *Equivalent circuit used to represent the fabricated OTFTs in BGBC configuration under analysis.*

The circuit was derived using MATLAB program, in order to obtain curves of real and imaginary components of the admittance as a function of the signal frequency which were the most possible similar to those obtained during the measurements, paragraph V.1.1. The characteristic time constants

are related to the physical processes occurring in the device. In particular, the capacitance values can be directly linked with the trap density involved in the fabrication processes, while the relaxation time constants give information about the energetic depth of the trap states. The proposed model consists in the series/parallel combination of five parameters: a capacitance due to the overlapping between the source and drain electrodes with the gate contact i.e. the silicon substrate (C_C), a capacitance rising from the overlapping of the channel region with the substrate (C_{ch}), the channel resistance (R_{ch}), an admittance (Y_t) due to the traps in the semiconductor bulk, and a contact resistance measured at the electrodes (R_C).

The contribution of each layer of the device is shown in Figure 50, where 4 main blocks are indicated.

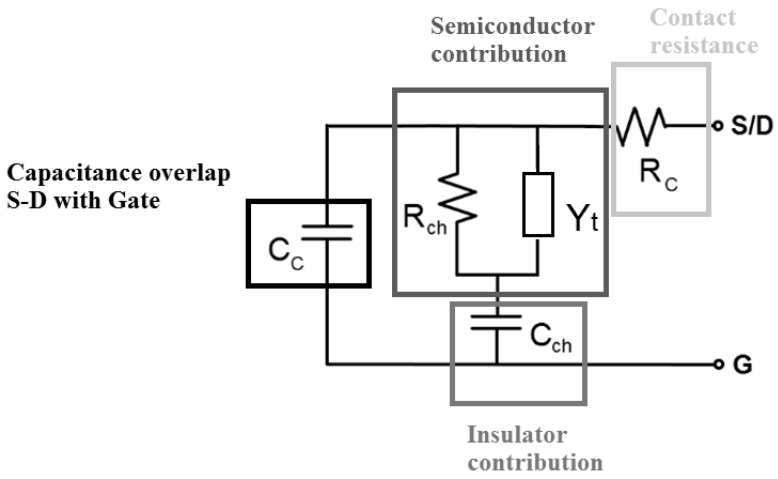


Figure 50: *Representation of the contributions of the layers that make up the sample. The equivalent circuit is organized in four blocks: capacitance of overlap between S-D and gate electrode, semiconductor contribution, insulator contribution and contact resistance.*

The bottom-contact configuration of the fabricated devices yields the presence in the model of a capacitor defined by the overlapping between the source and drain electrodes with the silicon substrate. This capacitance is referred to as C_C and is given by:

$$C_C = \varepsilon_0 \varepsilon_i \frac{A_C}{t_i}, \tag{27}$$

where ε_0 is the vacuum permittivity, ε_i is the dielectric constant of silicon dioxide, A_C is the source and drain electrode area (including the contact pads) and t_i is the insulator thickness. The capacitance of overlap is measured directly from the samples. This contribution is common to all the devices and is constant and equal to 650÷700 pF.

In parallel to the capacitor of overlap, it is present the semiconductor contribution. In particular, the channel region, which is formed at the interface with the insulator, is described by the channel resistance R_{ch}, whereas the bulk region is represented through the admittance of traps Y_t. The channel resistance contains the information on the channel formed in the semiconductor and on the trap levels formed at the interface at low frequency. Considerations on the admittance of the traps will be detailed in the following paragraphs, where two different interpretations will be given. The channel resistance obviously varies with the gate bias; while, from the observation of the admittance characteristics, the contribution of the admittance associated with the bulk traps is present at intermediate frequency and the bulk parameters result to be almost constant.

A further capacitive contribution is given by the insulator interposed between the semiconductor film and the gate contact, referred to as C_{ch} and defined as:

$$C_{ch} = \varepsilon_0 \varepsilon_i \frac{A_{ch}}{t_i}, \tag{28}$$

where A_{ch} is the area covered by the semiconductor film. This component gives its contribution at intermediate frequency in the analysis of the admittance measurements.

Finally, a contact resistance R_C is considered as further contribution. The effect of a contact resistance, in a bottom contact configuration, is due to the enhanced disorder in the deposited semiconductor. This resistance is added in series to the equivalent circuit to take into account the effect of the contacts at very high frequency.

V.4. Models of the Bulk Traps Admittance

The electrical response of the devices at an AC signal as a function of the DC bias is usually interpreted by the Shockley-Read-Hall (SRH) model (Nicollian & Brews, 2002), even if this is often considered unsuitable to organic semiconductors.

During this work of thesis, the admittance measurements are analyzed considering the equivalent circuit extracted, and using two different expressions of the admittance associated with the traps (Nicollian & Brews, 2002).

Initially, to represent the admittance, it was considered a model where the traps occupy a single level. Relating this admittance contribution to the

measured admittance, it is possible to calculate some interesting parameters, as the density of the trap level, the channel resistance and the relaxation time of the bulk trap level. These parameters provide relevant information to investigate the quality of the semiconductor/insulator interface for the different fabricated devices. Then, in a second step, it was considered a model of distribution of single trap levels for a more realistic case. In this model, the equivalent trap admittance results more complex than the model of single trap level. Also in this case, some characteristic parameters of the devices can be found, that allow to compare the three types of devices under study.

V.4.1. Single trap level - Data Fitting

The model of a single trap level is based on the assumption that all the traps have the same energy level, i.e. all the traps are identical (Nicollian & Brews, 2002). By this simplification, the expression of the admittance for the traps $Y_t(\omega)$, considering a discrete energy level for the traps in the semiconductor bulk, is represented by the series combination of trap capacitance $C_t(\omega)$ and trap resistance $R_t(\omega)$. $C_t(\omega)$ is proportional to the density of the trap states, while $R_t(\omega)$ is the resistance to recombination. Their product depicts the relaxation time of the bulk trap level ($\tau_t = C_t(\omega)R_t(\omega)$).

This representation of $Y_t(\omega)$ has the same physical significance of the parallel model $Y_{eq}(\omega)=G_{eq}(\omega)+j\omega C_{eq}(\omega)$, where $G_{eq}(\omega)$ and $C_{eq}(\omega)$ are respectively the equivalent trap conductance and capacitance. In Figure 51 it is shown the equivalence of the two circuital representations.

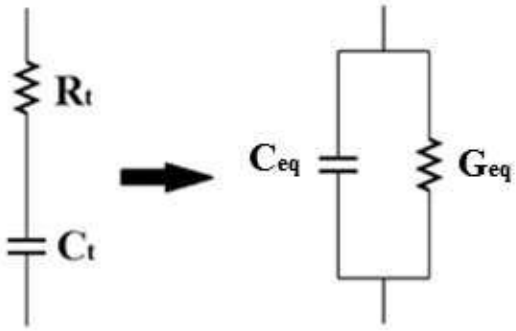


Figure 51: *Representation of the two equivalent circuits of $Y_t(\omega)$for the model of a single trap level. On the left-side, it is represented the series combination R-C network, and on the right-side, the parallel combination R-C network.*

The analogy is here demonstrated. The equivalent admittance is equal to:

$$Y_{eq}(\omega) = j\omega C_{eq}(\omega) + G_{eq}(\omega) = \\ = j\omega C_{eq}(\omega) + \omega\left(\frac{G_{eq}(\omega)}{\omega}\right) = \\ = \omega\left(jC_{eq}(\omega) + L_{eq}(\omega)\right), \tag{29}$$

where $L_{eq}(\omega)=G_{eq}(\omega)/\omega$ is the loss associated to the trap states.

The admittance for the traps related to the first circuital representation is equal to:

$$Y_t(\omega) = \left(R_t(\omega) + \frac{1}{j\omega C_t(\omega)}\right)^{-1} = \\ = \frac{j\omega C_t(\omega)}{1 + j\omega R_t(\omega) C_t(\omega)}. \tag{30}$$

Multiplying and dividing everything by factor $(1-j\omega R_t(\omega)C_t(\omega))$,it is obtained:

$$Y_t(\omega) = \frac{j\omega C_t(\omega)\left(1 - j\omega R_t(\omega) C_t(\omega)\right)}{1 + \omega^2 (R_t(\omega) C_t(\omega))^2}. \tag{31}$$

Considering the relaxation time of the bulk trap level τ_t as the product of trap capacitance and trap resistance, the eq.(31) can be rewritten as:

$$Y_t(\omega) = \frac{j\omega C_t(\omega)}{1 + \omega^2 \tau_t^2} + \frac{\omega^2 \tau_t C_t(\omega)}{1 + \omega^2 \tau_t^2}. \tag{32}$$

The eq.(32) is the expression of the equivalent admittance considering a discrete energy level for the traps in the semiconductor bulk. The definitions of $C_{eq}(\omega)$ and $G_{eq}(\omega)$are derived from this equation as:

$$C_{eq}(\omega) = \frac{C_t(\omega)}{1 + \omega^2 \tau_t^2}, \tag{33}$$

$$G_{eq}(\omega) = \frac{\omega \tau_t C_t(\omega)}{1 + \omega^2 \tau_t^2}. \tag{34}$$

The plots of $C_{eq}(\omega)$ and $G_{eq}(\omega)/\omega$ vs. the product of the angular frequency and the relaxation time of the trap level ($\omega\tau$) are shown in Figure 52, from which it is possible to notice the analogy with admittance curves reported in paragraph V.1.1. Analyzing the graph, considering the behavior of the capacitance in response to the AC gate voltage, it is observed, at low values of $\omega\tau$ ($\omega\tau$-›0), that traps immediately change occupancy. As soon as $\omega\tau$ increases, traps change occupancy with a lag in response to the AC gate voltage, now no longer immediately. Increasing further $\omega\tau$ at very large

value ($\omega\tau$-›∞), trap occupancy changes very little in response to the AC gate voltage. Considering now the plot of the energy loss in response to the AC gate voltage: at low $\omega\tau$, there is no energy loss because $G_{eq}(\omega)/\omega \approx 0$,but as soon as $\omega\tau$ increases, an energy loss is produced, because traps lag behind the AC gate voltage. Then, increasing $\omega\tau$, $G_{eq}(\omega)/\omega$ increases until $\omega\tau$=1, where $G_{eq}(\omega)/\omega$ reaches a peak value. In this point, the energy loss matches half the level of the corresponding capacitance. Increasing further $\omega\tau$, some traps do not respond at all, so the $G_{eq}(\omega)/\omega$ decreases from its peak value. Finally, at very large values of $\omega\tau$, traps hardly change occupancy. So, there is no longer any energy loss, and $G_{eq}(\omega)/\omega \approx 0$ again.

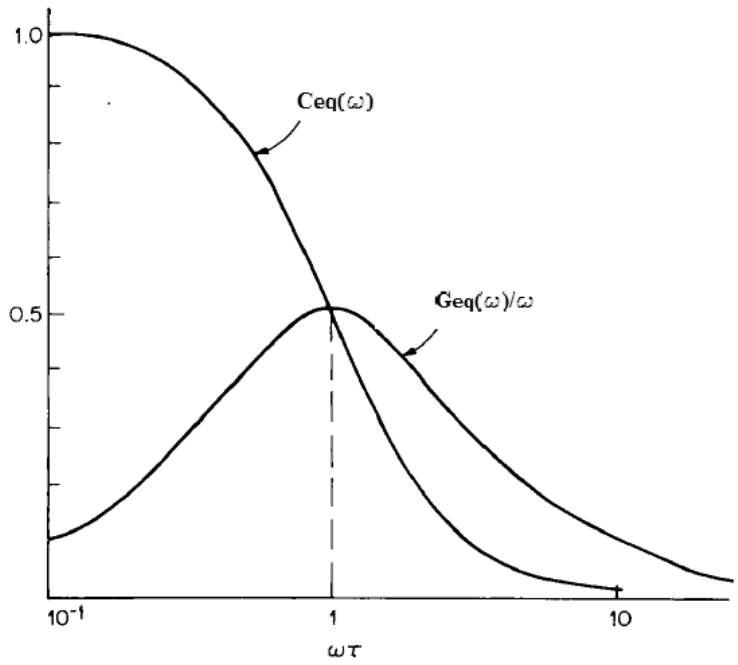


Figure 52: *Plots of equivalent trap capacitance $C_{eq}(\omega)$ and equivalent trap conductance $G_{eq}(\omega)/\omega$ as a functions of ωτ derived by eq.(33) and (34) according to the model of a single trap level.*

V.4.1.1. Experimental data fitting and extracted parameters

The expression of the admittance for the traps considering a discrete energy level for the traps in the semiconductor bulk is cumulative with the other contributions of the device described in the equivalent circuit. All these contributions together are used to extract from the experimental measurements the characteristic parameters of the devices under analysis.

The simulation of the equivalent circuit was studied for all the devices typologies, that is, the samples with processed HMDS at the three different temperatures. To calculate the parameters, some assumptions have been made:

a) the dielectric constant of the silicon dioxide ε_i is assumed 3.9;
b) the capacitance of the overlap of the source and drain contacts with the gate plate, being common to all the devices, is considered constant and equal to700 pF.

To illustrate the used procedure, the fitting results of the capacitance and of the loss as a function of the signal frequency are shown in

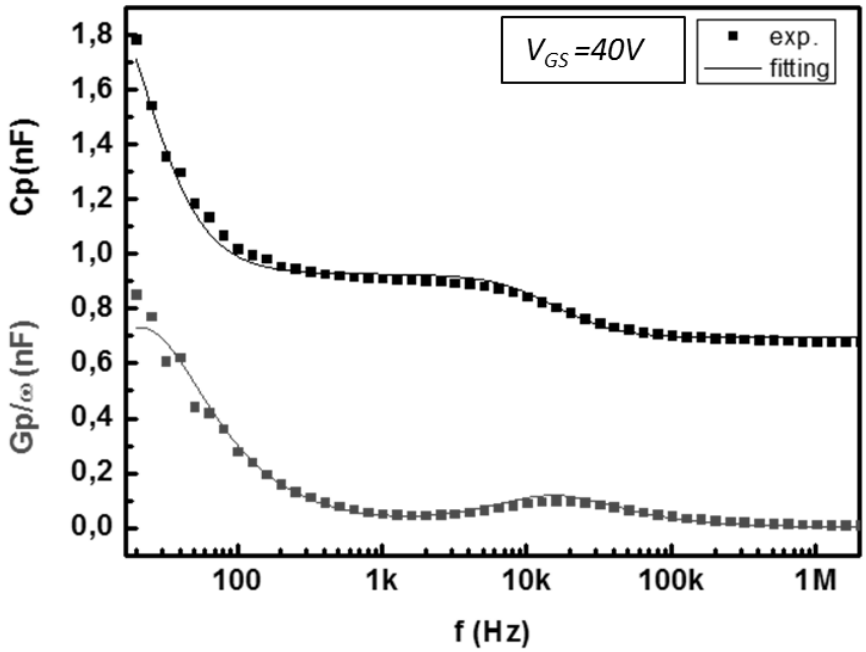


Figure **53** (linear scale) and Figure 54 (logarithmic scale), at V_{GS} = *40 V*, for a device with HMDS processed at 7°C.

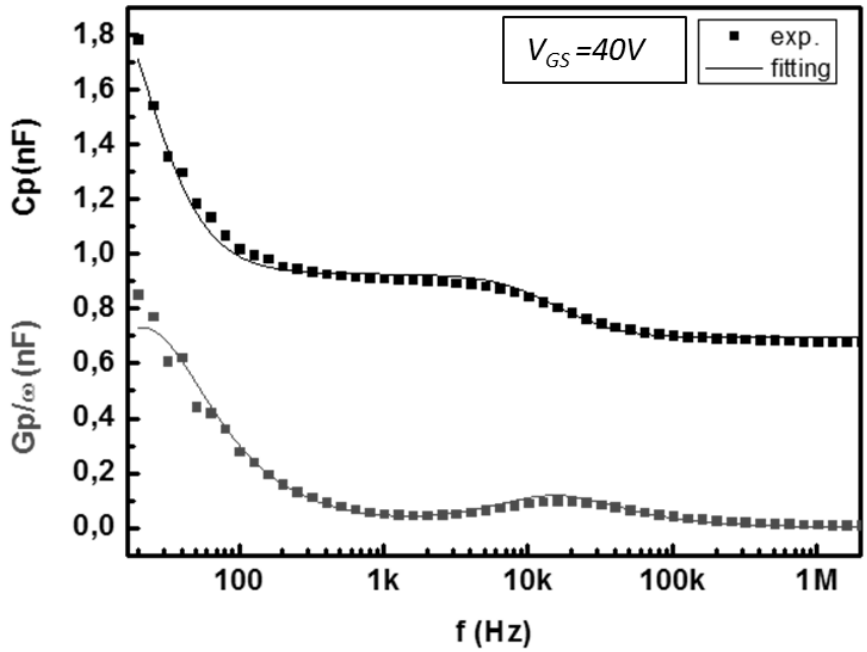


Figure 53: *Fitting of the experimental data measured at V_{GS} =40V (symbols) according to the model (lines) of single-level traps for the admittance of the traps for a sample with HMDS deposition temperature of 7°C. Linear scale for the admittance axis.*

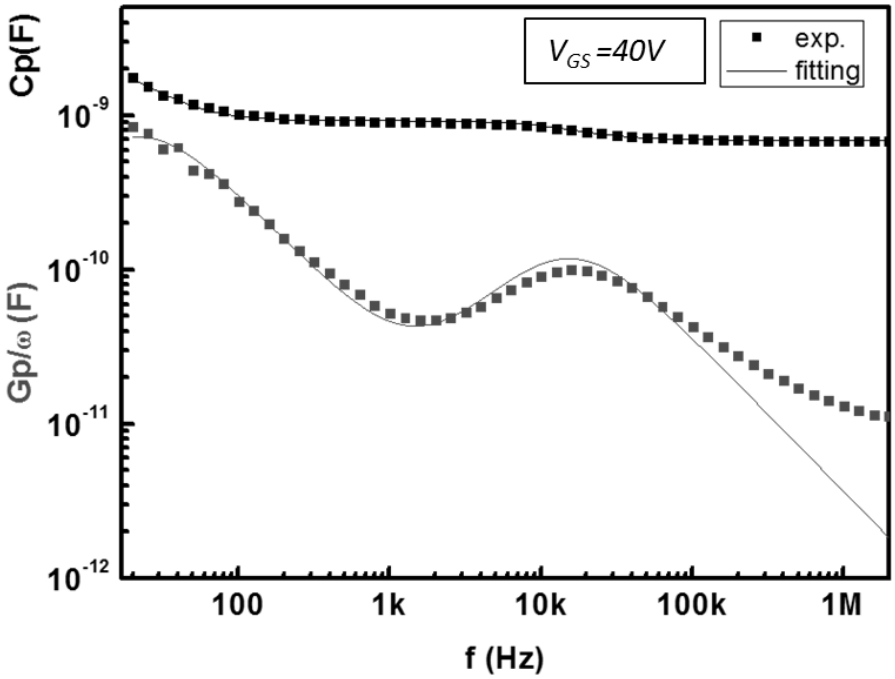


Figure 54: *Fitting of the experimental data at V_{GS} = 40V (symbols) according to the model (lines) of single-level traps for admittance of traps for the sample with HMDS deposition temperature of 7 °C. Logarithmic scale for admittance axis.*

The model shows good agreement for both the capacitance and the loss of the measured admittances. Fitted data allow extracting the values of the components of the equivalent circuit model, as well as the density of the bulk traps, the channel resistance and the relaxation time of the bulk trap level τ_t, for all the devices as a function of the HMDS deposition temperature. In Table 4 all the parameters of interest are reported.

Table 4*:Summary of all the components extracted from the experimental data at V_{GS} = 40 V according to the equivalent circuit. Extracted considering C_C = 700 pF*

CA(°)	HMDS dep. temp. (°C)	C_{ch}(nF)	R_{ch}(MΩ)	C_t(pF)
104.1	60	1.84±0.02	3.0±0.2	236±3
106.1	7	1.69±0.01	3.7±0.3	269±4
109.3	25	1.83±0.02	4.9±0.6	636±5

CA(°)	HMDS dep. temp. (°C)	τ_t(μs)	D_t (cm^{-3} eV^{-1})	A_{ch} (cm^{-2})
104.1	60	10.8±0.3	$1.62\pm0.01\cdot10^{16}$	0.11±0.01
106.1	7	11.8±0.4	$1.96\pm0.01\cdot10^{16}$	0.10±0.01
109.3	25	36.4±0.5	$4.09\pm0.04\cdot10^{16}$	0.12±0.01

The density of the trap states D_t is a relevant parameter and can be calculated from C_t (Nicollian & Brews, 2002) as:

$$D_t = \frac{C_t}{qA_{ch}d_{osc}\left(\frac{kT}{q}\right)}, \tag{35}$$

where d_{osc} is the thickness of the organic semiconductor and its value is equal to 300 nm, while kT/q is equal to 25.8 mV. The semiconductor area A_{ch} is calculated as the ratio of the channel capacitance with the capacitance of overlap, in the following way:

$$A_{ch} = A_c\frac{C_{ch}}{C_c} \tag{36}$$

where the source and drain electrode area A_c is constant for all devices and equal to 0.045 cm^2.

The R_{ch} and D_t are plotted versus the contact angle measured in Figure 55. From Figure 55, it can be observed that both the channel resistance R_{ch} exhibited by the semiconductor at the interface with the insulator, and the traps density in the semiconductor bulk D_t increase with the contact angle of the treated substrate surface on which the semiconductor layer is deposited. This growth means that the increase of the hydrophobicity of the semiconductor/insulator interface for BCBG devices leadsin an increase of the number ofthe traps which induce a decrease of the charge carriersthat contribute to the drain current, for a fixed bias, resulting in a reduction of the OTFTs performance, i.e. higher V_T and lower mobility.

The HMDS deposition at room temperature, which gives the higher contact angle, represents the worst condition for the semiconductor quality; while the deposition at 60 °C, which yields the smallest contact angle, assures less trap states. These results confirm the evidences already met in the DC analysis, of a better quality of the semiconductor/insulator interface resultant from the HMDS treatment at temperature of 60 °C.

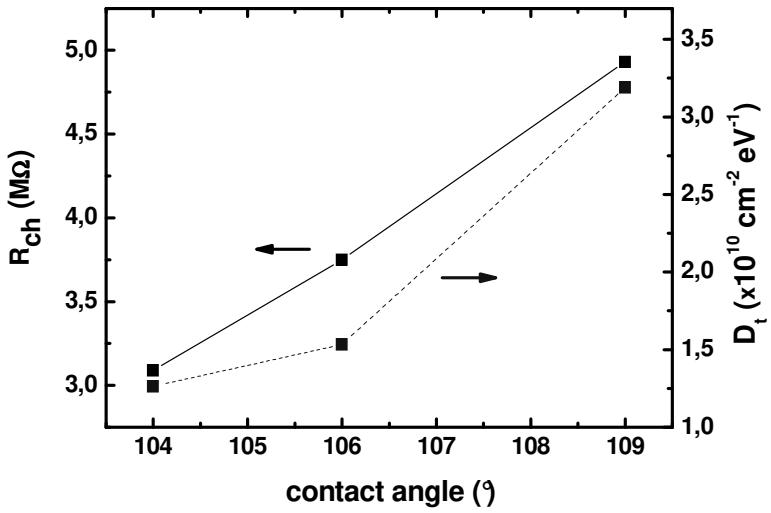


Figure 55: *Channel resistance R_{ch} (solid line) and density of the trap states D_t (dashed line) vs. the contact angle of the surfaces of the samples treated at the different HMDS deposition temperatures.*

Anyway, observing the fit of the measured data in Figure 55, this model doesn't succeed in well reproducing the loss at higher frequency. In this zone, the measured data show the tail of a resonant peak at higher frequencies, which is due to the contact resistance. For this reason, a more accurate model has been studied.

V.4.2. Distribution of single trap levels- Data Fitting

Instead of considering a single level for the traps, we now assume there is a distribution of several single levels. This model gives a further interpretation of the trap levels. From intuitive considerations on the trap levels, if we deal with many trap levels, they are so close in energy in the organic semiconductor bandgap that they cannot be distinguished as separate levels. However, trap levels do not form a continuous band because trap sites are spatially too far apart, and the wave functions of the electrons localized on neighboring traps don't overlap. Therefore, transitions occur only between the trap levels and the semiconductor bands in an interval a few *kT* around surface Fermi level (E_F), and not directly between trap levels on different sites, even if the levels are near in energy (Nicollian & Brews, 2002). So, the bulk traps are located in the depletion layer where the trap levels cross the Fermi level. Their response at the AC signal depends on the AC band bending at the crossover point, Figure 56. Each trap level in the

energy interval kT wide around E_F contributes a different energy loss, depending on its distance in energy from the E_F

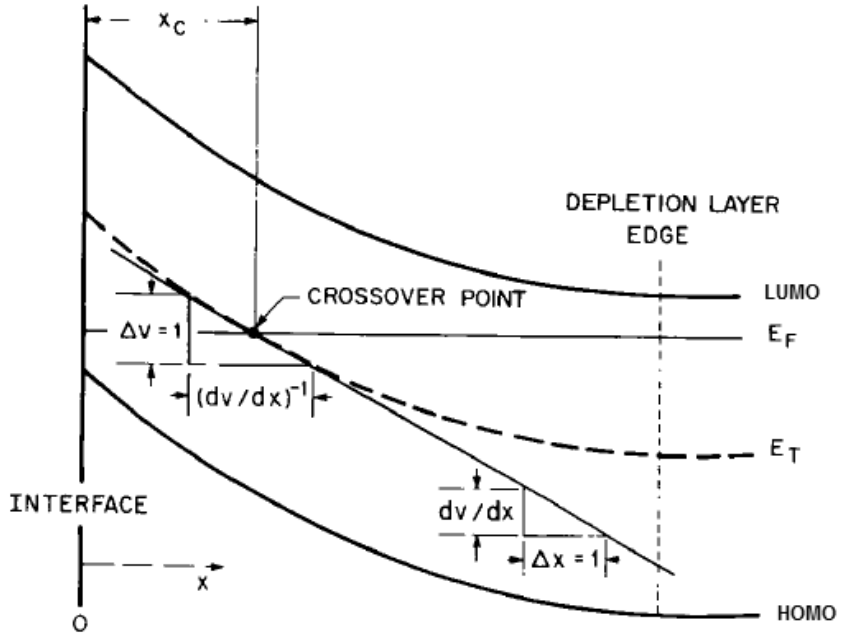


Figure 56: *Representation of the band bending vs distance from the interface into the organic semiconductor. E_T is the bulk trap level (dashed line), while E_F is the Fermi Level (solid line).This diagram shows that bulk traps are active in a region of width $(dv/dx)^{-1}$ near the crossover point, that corresponds to the region where bulk trap levels are within kT/q of the Fermi level.*

For a distribution of single trap levels, the equivalent circuit in the depletion region becomes a parallel combination of C_{eq}-G_{eq} branches with one branch for each level.

According to this model Nicollian&Brews, the equivalent traps admittance is dominated by the losses due to the delay between capture and emission of the electrons by the bulk trap levels at intermediate frequencies. The crossover admittance, in this frequency range, is represented Nicollian&Brews as:

$$Y_{eq}(\omega) = j\omega C_{Tn} = \frac{C_{bt}}{\tau_n}\left\{j\arctan(\omega\tau_n) + \frac{1}{2}\ln[1+(\omega\tau_n)^2]\right\} \quad (37)$$

$$Y_{eq}(\omega) = \frac{C_{bt}}{\tau_t}\left\{j\arctan(\omega\tau_t) + \frac{1}{2}\ln[1+(\omega\tau_t)^2]\right\}$$

where C_{Tn} is the so-called crossover capacitance related to bulk traps levels that crossing the Fermi level. C_{bt} is the capacitance of the number of the bulk trap levels D_{bt} per unit area within kT/q of the crossover and τ_n is the capture time for the electrons at crossover. The density of the trap states D_{bt} is now given by the relation:

$$D_{bt} = \frac{C_{bt}}{qA_{ch}d_{osc}\left(\frac{kT}{q}\right)}, \quad (38)$$

where d_{osc} is the thickness of the organic semiconductor and A_{ch} is the contact area. The equivalent parallel capacitance C_{eq} and conductance G_{eq} for the semiconductor are extracted from the eq.(37) and defined to be:

$$C_{eq}(\omega) = \frac{C_{bt}}{\omega\tau_n}\arctan(\omega\tau_n), \quad (39)$$

$$\frac{G_{eq}(\omega)}{\omega} = \frac{C_{bt}}{2\omega\tau_n}\ln[1+(\omega\tau_n)^2]. \quad (40)$$

where the real component of the equivalent trap admittance increases along with the frequency.

The two models used to interpret the traps admittance are compared in Figure 57 and Figure 58, where capacitance and loss are shown for the model of a single trap level (dashed curve) and for the model of a distribution of single trap levels (solid curve). For first model the equation used are eqs. (33) and (34), for capacitance and loss respectively. While for the model of a distribution of single trap level eqs. (39) and (40) are used. The behavior of the capacitance and the loss vs. $\omega\tau$ for both the models is qualitatively very similar. In the case of the model of a distribution of single trap levels, capacitance and conductance curves are broader along the $\omega\tau$ axis. In fact, the loss peak is now shifted from $\omega\tau_t$=1 to $\omega\tau_n$=1.98 and its magnitude value results $G_p/\omega = 0.4qD_{bt}$ (Nicollian & Brews, 2002).

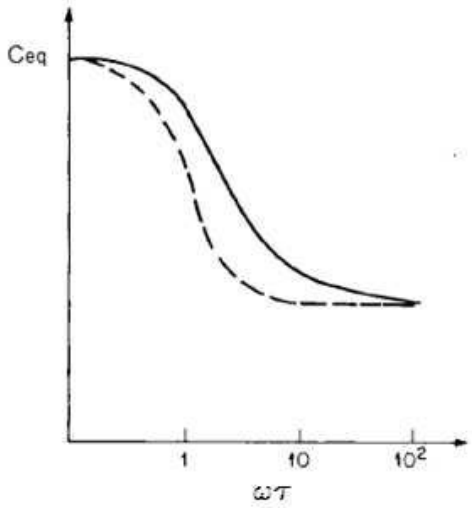


Figure 57: *Plots in logarithmic scale of the equivalent trap capacitance $C_{eq}(\omega)$ vs. $\omega\tau$ for the model of a single trap level (dashed curve)as derived from eq. (33) and for the model of a distribution of single trap levels (solid curve)as derived from eq. (39).*

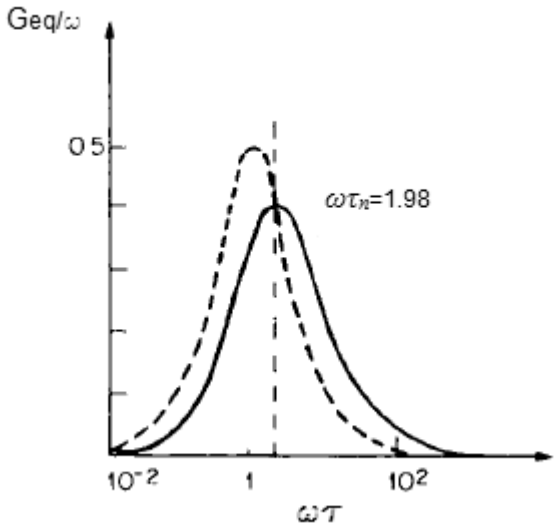


Figure 58: *Plots in logarithmic scale of the equivalent trap conductance $G_{eq}(\omega)/\omega$ vs. $\omega\tau$ for the model of a single trap level (dashed curve) as derived from eq. (34) and for the model of a distribution of single trap levels (solid curve) as derived from eq. (40). The maximum for the distributed trap levels is at $\omega\tau_n$=1.98.*

V.4.2.1. Experimental data fitting and extracted parameters

The simulation of equivalent circuit using the model of a distribution of single trap level for the equivalent trap admittance is studied for all samples with the three different HMDS deposition temperatures. For calculate the parameters are made some assumptions. As for the model of single traps level, the dielectric constant of silicon dioxide ε_i is assumed to be equal to 3.9, the capacitance of overlap is considered common, constant and equal to 700 pF, and the semiconductor area A_{ch} calculated as in eq.(36).

Now, the contribution of the semiconductor is discussed with more detail, to give a more accurate analysis. Because of its drop-shape, the channel resistance can be approximated as the resistance of a series of infinitesimal annular rings, each having a width of $d\rho$ and a resistance of $(R_{ch,sh}/2\pi\rho)d\rho$, where $R_{ch,sh}$ is the channel sheet resistance and ρ is the resistivity of the organic semiconductor. The resistance is calculated as the integral over all such annular rings, with the larger circle of radius equal to the drop radius, r_2,andthe smaller one equal to the radius r_1. The radius r_2 is estimated from the evaluation of A_{ch}, while the smaller one is given by the area covered by the interdigitated contacts, estimated as a circle of radius r_1, assuming negligible the channel region between the interdigitated contacts with respect to the total semiconductor area. Solving the integral formula of resistance, the expression of the channel resistance is now equal to:

$$R_{ch} = \frac{R_{ch\_sh}}{2\pi} \ln \frac{r_2}{r_1} \tag{41}$$

From eq. (41) it is possible to obtain the value of the channel sheet resistance $R_{ch,sh}$. This is an important parameter, extracted from the measurements, to analyze the different samples. The sheet resistance is a measure of the resistance of the thin films, and it is used to compare the electrical properties of devices that are different in size. Furthermore, it is invariable under scaling of the deposited film. Its expression is:

$$R_{ch\_sh} = \frac{\rho_{ch}}{t_{ch}} \tag{42}$$

where ρ_{ch} and t_{ch} are respectively the resistivity and the thickness of the accumulation channel region.

The fitting results of capacitance and loss, using the electrical model and plotted vs. the signal frequency, are shown in Figure 59 (linear scale) and Figure 60 (logarithmic scale), for different gate voltage, for the devices type with HMDS processed at 7°C.

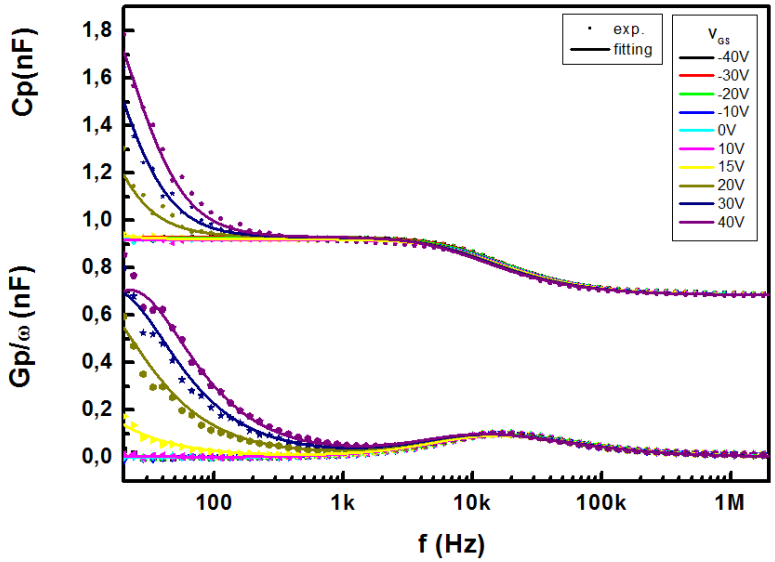


Figure 59: *Fit of the experimental data, measured at different V_{GS} (symbols), according to the model (lines) of the distribution of single trap levels for the admittance of the traps for the samples with HMDS deposition temperature at7°C. Linear scale for the admittance axis.*

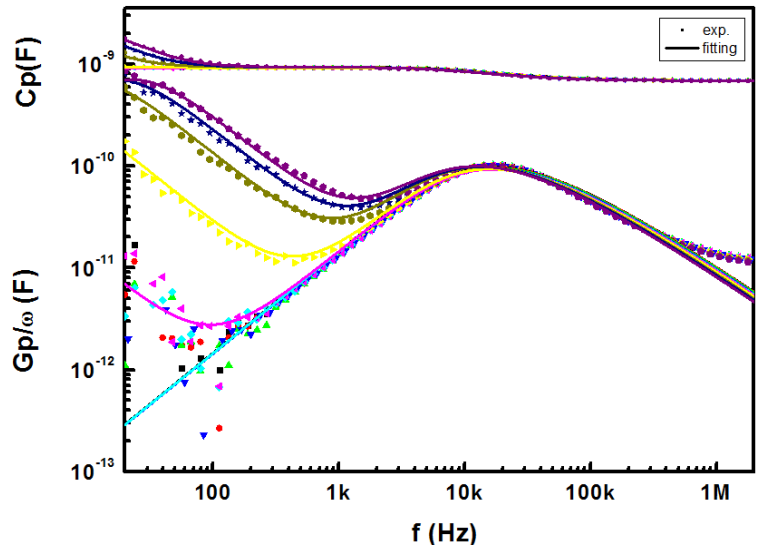


Figure 60: *Fit of the experimental data, measured at different V_{GS} (symbols), according to the model (lines) of the distribution of single trap levels for the admittance of the traps for the samples with HMDS deposition temperature at 7°C. Logarithmic scale for the admittance axis.*

From the fit, it is possible to observe that the model of the distribution of single trap levels shows good agreement with the experimental data, for both the capacitance and the loss of the measured admittance, and allows to extract the values of each component for all the voltages. This model of the traps admittance is more accurate than the model of single-level traps. This consideration derives from the analysis of the adjusted r-squared R^2_{adj} (Ohtani & Tanizaki, 2004). The adjusted r-squared provides a measure of how well observed outcomes are replicated by a model, based on the proportion of total variation of outcomes explained by the model. The coefficient of determination ranges from 0 to 1. When the coefficient R^2_{adj} is zero, the applied model does not explain at all the experimental data, while if it is one the model explains the data perfectly.

The minimum value of the adjusted r-squared for the model of single-level traps for all samples is resulted equal to 0.997, while for the model of the distribution of single trap levels, the adjusted r-squared never drops below 0.999. For this reason, the second model can be considered more faithful than the other one.

The parameters extracted from the model using the distribution of single trap levels are reported in Table 5 for all the three HMDS deposition temperatures. Among the various parameters, noteworthy are the sheet channel resistance, the density of the bulk states and the relaxation time of the bulk trap level, which are plotted vs. the contact angle in Figure 61.

Table 5*: Summary of all the components extracted from the experimental data at V_{GS} = 40 V according to the equivalent circuit. Extracted considering C_C about 700 pF.*

CA(°)	HMDS dep. temp. (°C)	R_{ch}(MΩ)	C_{bt} (pF)	τ_t(μs)
104.1	60	2.9±0.1	298.2±2.8	23.8±0.1
106.1	7	3.6±0.1	286.0±1.7	29.3±0.1
109.3	25	4.8±0.5	690.3±3.9	93.4±1.6

CA(°)	HMDS dep. temp. (°C)	D_{bt} (cm^{-3} eV^{-1})	C_{ch} (nF)
104.1	60	$1.48\pm0.01\cdot10^{16}$	2.77±0.08
106.1	7	$2.38\pm0.01\cdot10^{16}$	1.85±0.04
109.3	25	$5.14\pm0.03\cdot10^{16}$	1.65±0.02

CA(°)	HMDS dep. temp. (°C)	R_{ch_sh} (MΩ)	A_{ch} (cm^{-2})
104.1	60	1.84±0.06	0.16±0.01
106.1	7	1.69±0.04	0.09±0.01
109.3	25	1.83±0.09	0.10±0.01

The channel resistance values are similar to the ones from the first model, and high enough to prevent spurious current paths between source and drain when the drops of the semiconductor could extend outside the interdigitated contacts, so these values can be referred only to the contributions due to the channel. The variability of these drops can also explain the different values of the semiconductor area.

It is evident how the samples at 25°C show much worse values than the other devices. And this trend is clearly visible in Figure 61. From the AC data, it appears that these were the worst conditions of treatment, because these devices show an increase of the traps in the organic semiconductor.

The values of the density of the trap bulk states, D_{bt}, for all the gate voltages applied at the samples are shown in, Figure **62**. In depletion regime, the D_{bt} is almost constant, with very small variations with the bias. In accumulation regime, when the threshold voltage is reached and above, there is just a small increase: this means that few new trap states are induced by the bias, and their largest quantity was generated during the deposition of the material.

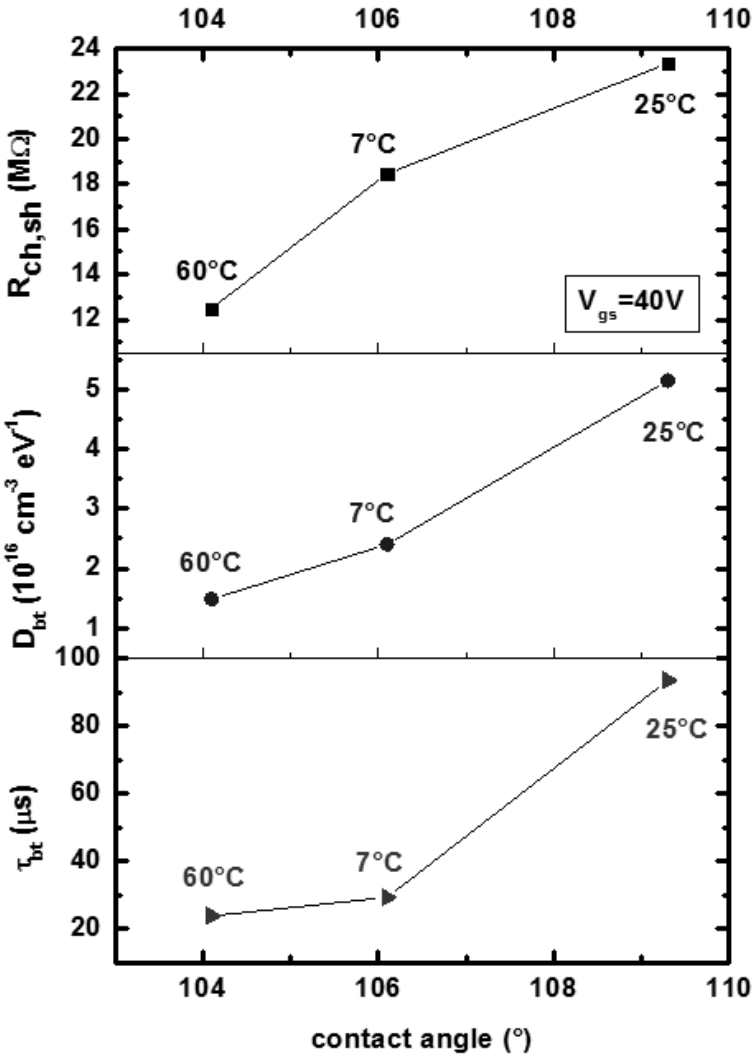


Figure 61: *Sheet channel resistance (R_{ch_sh}), density of the trap states (D_{bt}) and the relaxation time of the bulk trap level (τ_{bt}), calculated from the data measured at V_{GS} = 40 V, vs. the contact angle of the surfaces of the samples treated at the different HMDS deposition temperatures, according to the model of the distribution of single trap levels.*

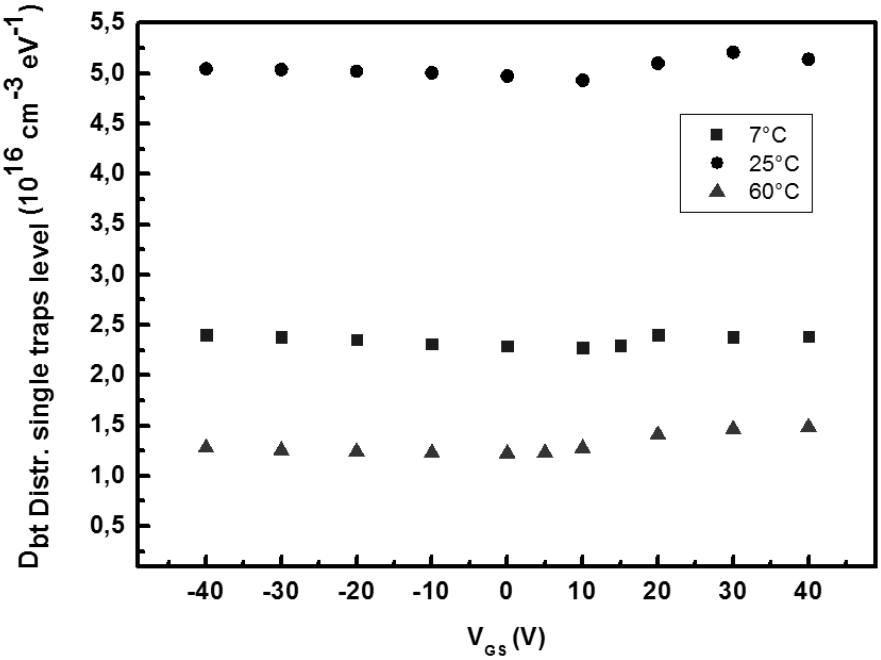


Figure 62: *Trend of the density of the trap states (D_{bt}) as a function of the applied gate voltage (V_{GS}), for all the samples treated at the different HMDS deposition temperatures (7°C, 25°C, 60°C).*

V.4.3. Comparison between the models of single-level traps and of distribution of single trap-levels

In this thesis, two models for the interpretation of the traps admittance have been employed: the model of single-level traps, which can be considered a simplification of the traps behavior, as all the traps are thought to have the same energy; and the model of a distribution of single trap levels, that considers many trap levels very closely spaced in energy in the organic semiconductor bandgap. These assumptions make the second model more realistic.

Furthermore, as previously said in the paragraph V.4.2.1, the two models here studied have been analyzed according to the adjusted r-squared R^2_{adj} method. From this statistical analysis, the second model resulted better than the other one.

From eq. (32) for the model of the single-level traps and from eq. (37) for the model of a distribution of single trap levels, the density of the trap states and the relaxation time of the bulk trap level can be derived.

For the first model, these values are calculated fitting one curve of the bias gate, in detail only for V_{GS} = *40V*, while for the second model the

parameters are calculated considering the concatenated data, in other words all data obtained for the different bias gate are used. So that, for this second model, the extracted parameters are referred to a larger number of experimental data, and the results can be considered more accurate, as also the statistical analysis revealed.

In Figure 63 the values of the densities of the trap states for the two cases are compared. The traps density in the semiconductor bulk for the model of single-level traps assumes values lower than the case of the distribution of single trap levels, with the exception of the samples to the lowest hydrophobicity, the samples fabricated with HMDS treatments at temperature of 60°C. The higher statistical reliability of the second model should produce more faithful data.

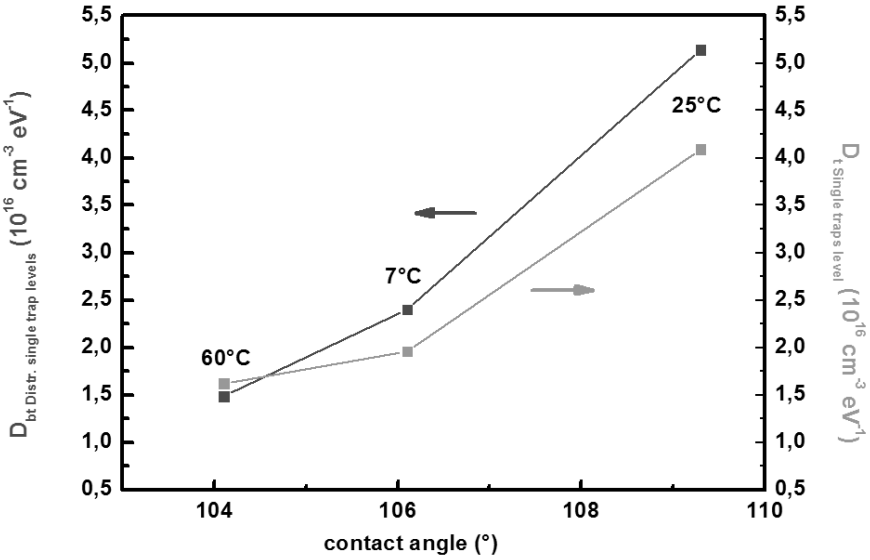


Figure 63: *Comparison of the density of the trap states for the model of single-level traps (line orange) and for the model of a distribution of single trap levels (line green, for V_{GS}= 40V.*

V.4.4. Comparison of DC vs.AC parameters

Lastly, the parameters of interest obtained from the DC measurements, as the charge carrier mobilityμ and the threshold voltage V_T, are compared with the density of the interface trap levels D_{bt} obtained from the AC measurements using the model of the distribution of single trap levels. All these parameters are dependant from the grade of hydrophobicity of the gate insulator surface, which depends on the different temperatures of the HMDS deposition process.

In Figure 64 the density of the interface trap levels and charge carrier mobility are shown. The highest mobility and thus the best device performance is found for the samples with the lower hydrophobicity, that is the samples realized with a HMDS temperature of 60°C. As expected, the lowest value of the density of the interface trap levels is found for the samples processed at 60°C.

Similarly, in Figure 65,the density of the interface trap levels and the threshold voltage vs. the contactangle are shown. A low threshold voltage indicates the best performance, and also for this case the lowest value is reached by the samplesprocessed at 60°C.

A low value of the trap states density allows that lower biases generate enough charges in the channel to completely fill the traps, and an easier movement of the charges in the channel when V_{DS} is applied, so for the devices prepared during this thesis, the results extracted from the I-V static measurements and from the AC measurements coherently confirm each other, and indicate that the samples with the HMDS prepared at 60°C gave the best level of hydrophobicity for the best OTFTs performance.

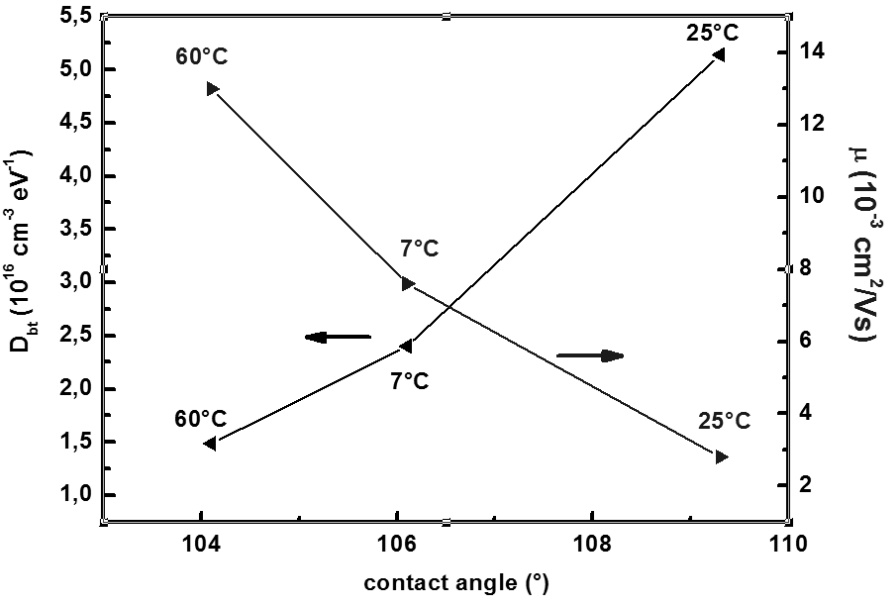


Figure 64: *Density of the interface trap levels D_{bt} and charge carrier mobility μ vs. the contact angle of the surfaces of the samples treated at the different HMDS deposition temperatures.*

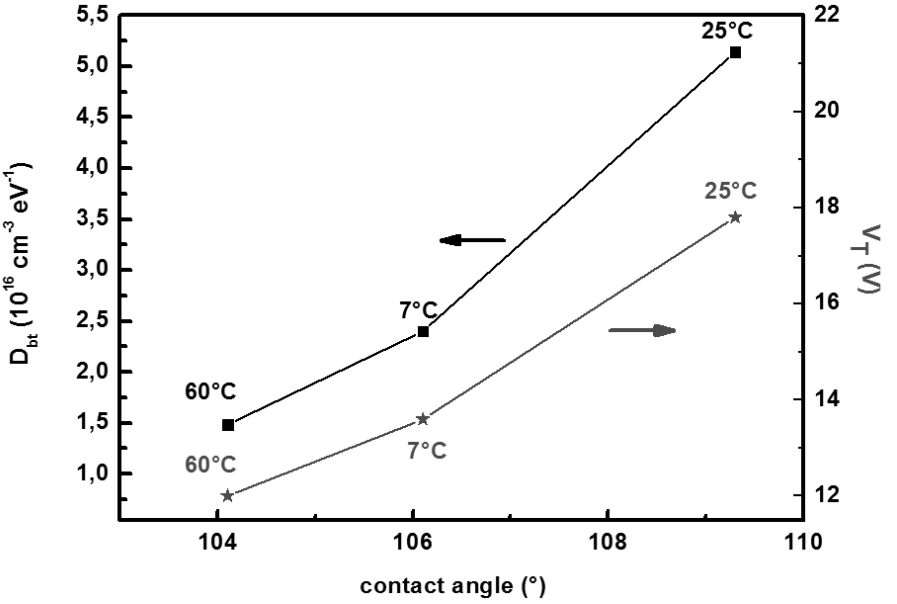


Figure 65: *Density of the interface trap levels D_{bt} and threshold voltage V_T vs. the contact angle of the surfaces of the samples treated at the different HMDS deposition temperatures.*

Conclusion

In this thesis, n-type organic thin film transistors in configuration BGBC were studied, focusing on the combination of different treatments of the insulator/semiconductor interface and studying their effects on the devices performances.

At first, it was evidenced that a two-steps combined scheme of UV/O_3 cleaning and HMDS treatment is beneficial for the performance of the $PC_{70}BM$-based OTFTs. Then, the influence of the temperature of the HMDS deposition was studied, as a pretreatment to vary the quality of the growth of the $PC_{70}BM$ films. From the combination of the observations from AFM analysis, DC measurements and admittance study, it is demonstrated that the temperature for the HMDS deposition is a sensible factor to influence the OTFTs performances.

By the AFM analysis, it was seen that a tailored hydrophobicity of the SAM is necessary for the formation of good $PC_{70}BM$ films, i.e., for BGBC OTFTs, a good matching of the dielectric surface energy with the semiconductor is a prerequisite to obtain good devices. In this thesis, the HMDS deposition at 60°C revealed as the best of the tested processes, inducing enough hydrophobicity of the dielectric to let the semiconductor grow with low surface roughness, and consequently probably with good crystallinity, which showed the best OTFTs performances, i.e. the higher mobility and the lower threshold voltage, as detected by the electrical parameters extracted from the I-V characteristics. HMDS depositions at 7°C and 25°C gave increasing hydrophobicity, but also higher roughness and worsening performances of the devices.

The AC analysis, namely the frequency response and the gate bias response of the admittance of the devices, led to the calculation of important parameters, like the density of the bulk traps levels and the channel resistance. In order to estimate the properties of the semiconductor and of the transistor conductive channel, an electrical equivalent circuit has been proposed that, for the first time here, analyzes the behavior of n-type OTFTs in a bottom-gate bottom-contact architecture. The proposed electrical model has been employed to interpret the experimental data of n-type OTFTs using two different models for the admittance associated with the traps: the model

of a single trap level, and the model of a distribution of single trap levels. The first model can be considered as a simplified version of the second one, which presents more stringent assumptions on the energy level of the traps. A statistical analysis of the results from the two model indicates that model of a distribution of single trap levels is more suitable to describe the observed AC behaviors of the devices.

However ,both these models showed that the devices treated with HMDS at temperature of 60°C have the lowest value of trap states, that, for the model of a distribution of single trap levels, assumes the value of $1.48 \cdot 10^{16} cm^{-3}\ eV^{-1}$. Remembering that typical density of deep trap states measured in the purest organic crystals, as anthracene or naphthalene crystals, are of the order of 10^{14}- $10^{15}\ cm^{-3} eV^{-1}$ (Kalb et al., 2010), the value here obtained can be considered a very good result.

Furthermore, by fitting the experimental data for the admittance measurements of the OTFTs, it was interesting to analyze the behavior of the loss $G_{eq}(\omega)/\omega$. The behavior of the loss is attributed to bulk traps associated with a distribution of single-level traps, the most accurate model applied here, according to a statistical analysis. Observing the results for all samples, it is possible to note that the magnitude of the peaks in the curves of $G_{eq}(\omega)/\omega$ vs. ω does not vary with the gate bias. It is due to a constant density of the bulk traps level with the traps depth, because of bulk traps would be deeper in the organic semiconductor. The same consideration is also valid for the frequency corresponding to the maxima of the loss, that does not vary with the gate bias. This frequency is dependent on the capture rates for the charge carriers near the point where the bulk trap levels cross the Fermi level. That means, the crossover point is always at the same distance from the depletion layer edge, so that the carrier density at crossover is always the same, independently of the gate bias. So that, the independence from the operating regime for the amplitude and the position of the resonance frequency of the peak for the loss curves can be reasonably attributed to a Fermi level pinning effect for the traps, that leads to a negligible variation of the band bending. The behavior of the density of bulk states was also evaluated as a function of the gate bias applied at the samples, and resulted approximately constant independently of the working regime. Also this behavior could justify a pinning effect.

In conclusion, all the observed behaviors, the values of the parameters extracted from the measured data and the evidences from the new prepared model reveal the importance to fine tailor the fabrication processes of n-type $PC_{70}BM$ OTFTs in bottom gate bottom contacts configuration, and in particular the treatments of the interface between the gate dielectric and the deposited semiconductor are critical to obtain good mobility and few traps in the transistor channel. Future steps of this work could deal with the use of other types of SAMs, with the use of an organic dielectric, with the stability of the devices performances versus various types of stress (bias stress,

thermal stress, light exposure, etc.), and with the application of the proposed model for other semiconductors.

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List of Symbols and Abbreviations

Symbols

A_C	electrode area
A_{ch}	area covered by the semiconductor
C	capacitance
C_C	contact capacitance
C_{ch}	channel capacitance
C_{eq}	equivalent trap capacitance
C_i	capacitance of the gate dielectric per unit area
C_t	trap capacitance
d_s	thickness of the semiconductor
D_t	density of the trap states
E_F	Fermi level energy
E_{tr}	single trap level energy
F	applied electric field
G	conductance
G_{eq}	equivalent trap conductance
g_m	transconductance
I_{on}/I_{off}	on/off current ratio
k	Boltzmann constant
L	length of the channel
$N_\square$	Total density of traps per unit area
n_o	free carrier density
q	elemental charge
Q	charge quantity
Q_o	intrinsic bulk charge
R_c	contact resistance
R_{ch}	channel resistance
$R_{ch,sh}$	channel sheet resistance
R_t	trap resistance
S	sub-threshold swing
T	absolute temperature

t_{ch}	thickness of the accumulation channel region
t_i	insulator thickness
V_T	threshold voltage
V_{fb}	flat-band voltage
V_{on}	onset voltage
W	width of channel
Y	admittance
Y_{eq}	equivalent trap admittance
Y_t	admittance of traps

β	dispersion parameter
β_{PF}	Poole-Frenkel slope
γ_{lv}	liquid-vapor interfacial tension
γ_{sv}	solid-vapor interfacial tension
γ_{sl}	solid-liquid interfacial tension
ε	dielectric constant
ε_0	vacuum permittivity
ε_i	dielectric constant of the insulator
θ_Y	Young's contact angle
μ	carrier field-effect mobility
μ_{LIN}	field effect mobility in linear regime
μ_{SAT}	field effect mobility in saturation
ρ_{ch}	resistivity of the accumulation channel region
σ	energetic disorder
τ	relaxation time
τ_n	capture time for the electrons at crossover relaxation time of
τ_t	the bulk trap level
ω	angular frequency

Abbreviations

AC	alternating current
Al	aluminum
Au	gold
BCB	benzocyclobutene
BGBC	bottom-gate bottom-contact geometry
C_{60}	fullerene
Ca	calcium
CA	contact angle
DC	direct current
HMDS	hexamethyldisilazane
HOMO	Highest Occupied Molecular Orbital

ITO	indium tin oxide
LUMO	Lowest Unoccupied Molecular Orbital
MIS	metal-insulator-semiconductor
N_2	nitrogen
OSC	organic semiconductor
OTFT	organic thin film transistors
$PC_{70}BM$	[6,6]-phenyl-C71-butyric acid methyl ester
SAM	self-assembled monolayer
SCA	static contact angle
Si	silicon
SiO_2	silicon oxide
UV/O_3	ultraviolet/ozone cleaning